Data Sheet, Rev. 1.12, October 2005

ADM6996L

6 Port Ethernet Switch Controller

ADM6996L, Version 1.0

Communication

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ADM6996L 6 Port Ethernet Switch Controller

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Previous Version: 1.05	
Page/Date	**Changed to the new Infineon format**
Sept./2004	**Rev. 1.1 changed to Rev. 1.11**
Oct./2005	**Rev. 1.11 changed to Rev. 1.12 for fixing pin type on page 15**

Trademarks

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1 Product Overview

1.1 Overview

The ADM6996L is a high performance, low cost, highly integration (Controller, PHY and Memory) five-port 10/100 Mbps TX/FX plus one 10/100 MAC port Ethernet switch controller with all ports supporting 10/100 Mbps Full/Half duplex. The ADM6996L is intended for applications to stand alone bridge for low cost SOHO market such as 5Port, Router application.

ADM6996L provides most advanced functions such as:**802.1p(Q.O.S.), 802.1q(VLAN), Port MAC address Locking, Management, Port Status, TP Auto-MDIX, 25M Crystal & Extra MII port** function to meet customer request on Switch demand.

The ADM6996L also supports Back Pressure in Half-Duplex mode and 802.3x Flow Control Pause packet in Full-Duplex mode to prevent packet lost when buffer full. When Back Pressure is enabled, and there is no receive buffer available for the incoming packet, the ADM6996L will issue a JAM pattern on the receiving port in Half Duplex mode and transmit the 802.3x Pause packet back to receiving end in Full Duplex mode.

The built-in SRAM used for packet buffer and address learning table is divided into 256 bytes/block to achieve the optimized memory utilization through complicated link list on packets with various lengths.

ADM6996L also supports priority features by Port-Base, VLAN and IP TOS field checking. User can be easy to set as different priority mode in individual port, through a small low-cost micro controller to initialize or on-the-fly to configure. Each output port supports four queues in the way of fixed N: 1 fairness queuing to fit the bandwidth demand on various types of packet such as Voice, Video and data. 802.1Q, Tag/Untag, and up to 16 groups of VLAN also is supported.

An intelligent address recognition algorithm makes ADM6996L to recognize up to 2048 different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by ADM6996L to use on Building Internet access to prevent multiple users sharing one port traffic.

1.2 Features

Main features:

- Supports five 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces and one MII/GPSI port.
- Supports 2048 MAC addresses table.
- Supports four queue for QoS
- Supports priority features by Port-Based, 802.1p VLAN & IP TOS of packets.
- Supports Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed.
- Supports buffer allocation with 256 bytes per block
- Supports Aging function Enable/Disable.
- Supports per port Single/Dual color mode with Power On auto diagnostic.
- Supports 802.3x Flow Control pause packet for Full Duplex in case buffer is full.
- Supports Back Pressure function for Half Duplex operation in case buffer is full.
- Supports packet length up to 1522 bytes.
- Broadcast Storming Filter function.
- Supports 802.1Q VLAN. Up to 16 VLAN groups is implemented by the last four bits of VLAN ID.
- 2bit MAC clone to support multiple WAN application
- Supports TP interface Auto MDIX function for auto TX/RX swap by strapping-pin.
- Easy Management 32bits smart counter for per port RX/TX byte/packet count, error count and collision count.
- Supports PHY status output for management system.
- 25M Crystal only for the whole system.
- 128 QFP package with 0.18um technology. 1.8 V/3.3 V power supply.

1.3 Applications

ADM6996L in 128-pin PQFP: SOHO 5-port switch
5-port switch + Router with MII CPU interface.

1.4 Block Diagram

Figure 1 below shows a simple block diagram of the ADM6996L internal blocks.

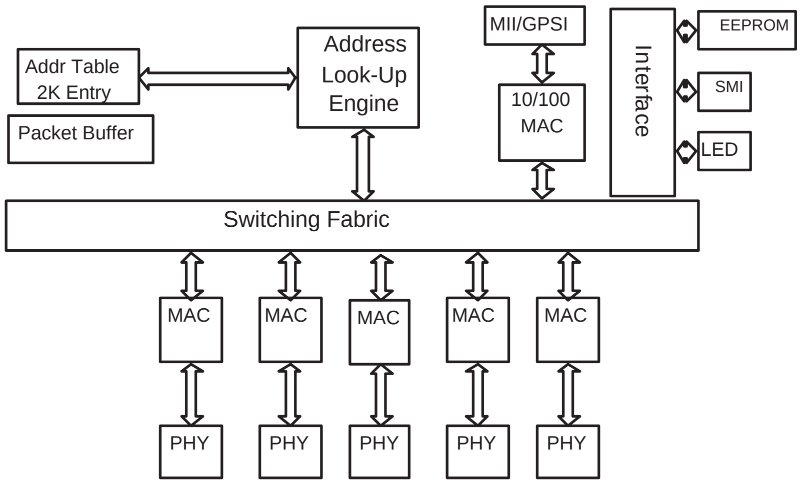

Figure 1 ADM6996L Block Diagram

2 Interface Description

This chapter describes the interface for the ADM6996L.

2.1 Pin Diagram

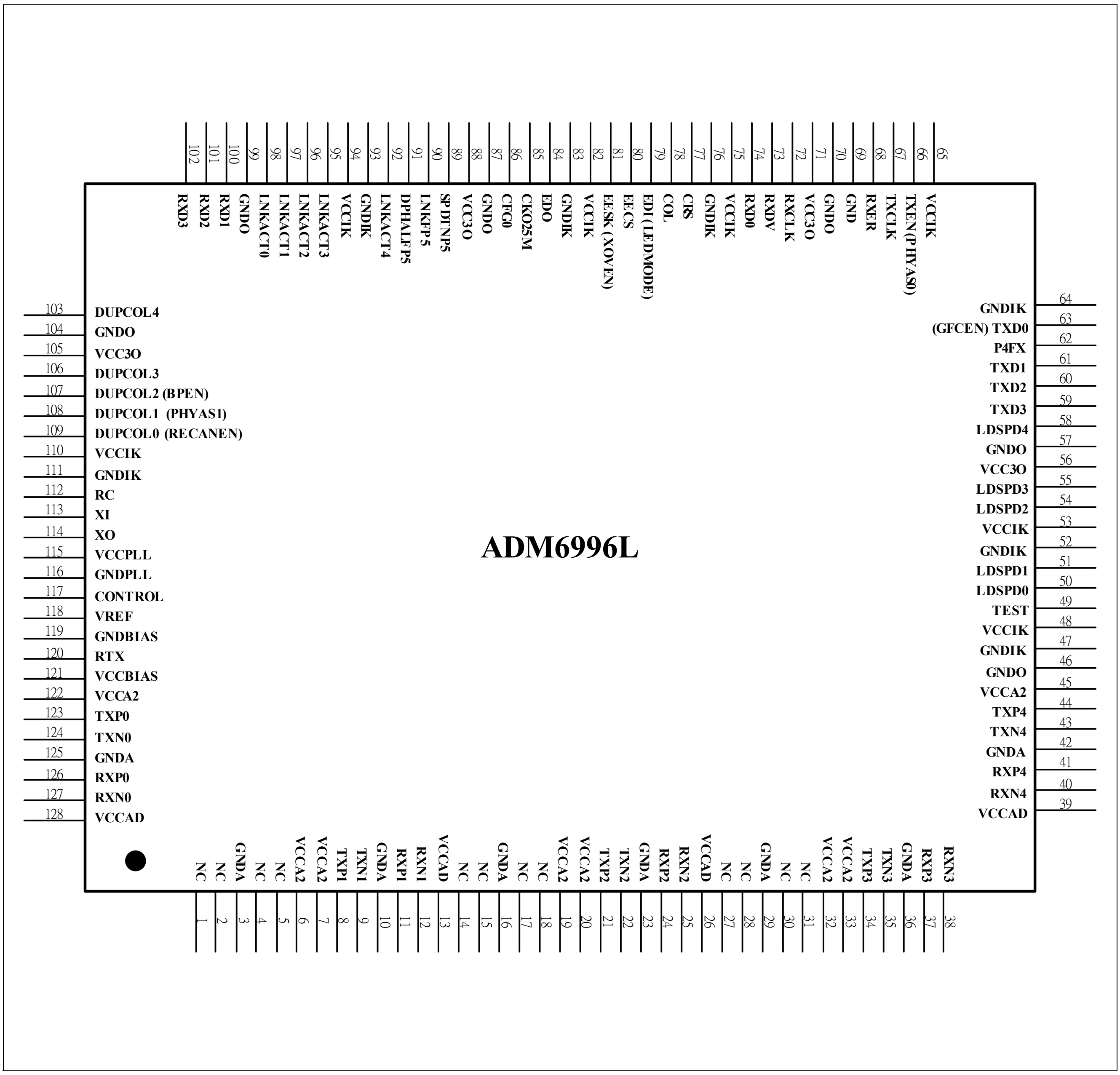

Figure 2 5 TP/FX PORT + 1 MII PORT 128 Pin Diagram

2.2 Pin Description by Function

ADM6996L pins are categorized into one of the following groups:

2.2.1 Twisted Pair Interface

Table 1 Twisted Pair Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
126	RXP0	AI/O		**Twisted Pair Receive Input Positive**
11	RXP1			
24	RXP2			
37	RXP3			
41	RXP4			
127	RXN0	AI/O		**Twisted Pair Receive Input Negative**
12	RXN1			
25	RXN2			
38	RXN3			
40	RXN4			
123	TXP0	AI/O		**Twisted Pair Transmit Output Positive**
8	TXP1			
21	TXP2			
34	TXP3			
44	TXP4			
124	TXN0	AI/O		**Twisted Pair Transmit Output Negative.**
9	TXN1			
22	TXN2			
35	TXN3			
43	TXN4			

2.2.2 6th Port (MII) Interfaces

Table 2 6th Port (MII) Interfaces

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
63	TXD[0]	I/O	8mA PU	**MII Tx Data bit 0/GPSI TXD** Acts as MII transmit data TXD[0]. Synchronous to the rising edge of TXCLK.
	SettingGFCEN	I/O	8mA PU	**Global Flow Control Enable** At power-on-reset, latched as Full Duplex Flow control setting“1” to enable flow-control (default), “0” to disable flow-control.

Table 2 6th Port (MII) Interfaces (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
61	TXD[1]	I/O	8mA PD	**MII Tx Data 1** Synchronous to the rising edge of TXCLK. These pins act as MII TXD[1].
	SettingP5GPSI	I/O	8mA PD	**SettingP5GPSI** Port 5 GPSI Enable. At power-on-reset, latched as P5 GPSI Enable."0" to disable port 5 GPSI (default), "1" to enable port 5 GPSI.
59	TXD3	I/O	8mA PD	**MII Tx Data bits 3** MII Transmit Data bit 3~2Synchronous to the rising edge of TXCLK. These pins act as MII TXD[3:2].
60	TXD2	I/O	8mA PD	**MII Tx Data bits 2** MII Transmit Data bit 3~2Synchronous to the rising edge of TXCLK. These pins act as MII TXD[3:2].
62	P4FX	I	PD	**Port4 FX/TX mode select** Internal pull down. 1_B **Port4 as FX port.**, 0_B **Port4 as TX port.**,
66	XEN	I/O	8mA PD	**MII Transmit Enable /GPSI TXEN** Internal pull down.
	SettingPHYAS0	I/O	8mA PD	**SettingPHYAS0** Chip physical address for multiple chip applications on read EEPROM data. Internal pull down.Power on reset value PHYAS0 combines with **PHYAS1PHYAS1 PHYAS00 0 Master(93C46)**
74	RXD0	I	PD	**MII port receive data 0 /GPSI RXD** This pin acts as MII RXD0. Synchronous to the rising edge of RXCLK. Internal pull down.
100	RXD1	I	PD	**MII port receive data 1** This pins act as MII RXD1. Synchronous to the rising edge of RXCLK. Internal pull down.
101	RXD2	I	PD	**MII port receive data 2** These pins act as MII RXD2. Synchronous to the rising edge of RXCLK. Internal pull down.
102	RXD3	I	PD	**MII port receive data 3** These pins act as MII RXD3. Synchronous to the rising edge of RXCLK. Internal pull down.
73	RXDV	I	PD	**MII receive data valid.** Internal pull down.
68	RXER	I	PD	**MII Port Receive Error.** Internal pull down.
78	COL	I	PD	**MII Port Collision input /GPSI Collision Input** Internal pull down.
77	CRS	I	PD	**MII Port Carrier Sense /GPSI Carrier Sense** Internal pull down.
72	RXCLK	I	PD	**MII Port Receive Clock Input /GPSI RXCLK**
67	TXCLK	I	PD	**MII Port Transmit clock Input /GPSI TXCLK**

Table 2 6th Port (MII) Interfaces (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
91	DHALFP5	I	PD	**Duplex** Internal pull down. 0_B , Full Duplex 1_B , Half Duplex
90	LNKFP5	I	PD	**MII Port Hardware Duplex input pin** MII Port Hardware Link input pin.Internal pull down. 0_B , Link OK 1_B , Link Off
89	SP D TNP5	I	PD	**MII Port Hardware Speed input pin** Internal pull down. 0_B , 100M 1_B , 10M

2.2.3 LED Interface

Table 3 LED Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
98	LNKACT0	O	8mA	**LINK/Activity LED0** Active low"1" indicates no link activity on cable"0" indicates link okay on cable, but no activity and signals on idle stage."Blinking" indicates link activity on cable.
97	LNKACT1	O	8mA	**LINK/Activity LED1** Active low"1" indicates no link activity on cable"0" indicates link okay on cable, but no activity and signals on idle stage."Blinking" indicates link activity on cable.
96	LNKACT2	O	8mA	**LINK/Activity LED2** Active low"1" indicates no link activity on cable"0" indicates link okay on cable, but no activity and signals on idle stage."Blinking" indicates link activity on cable.
95	LNKACT3	O	8mA	**LINK/Activity LED3** Active low"1" indicates no link activity on cable"0" indicates link okay on cable, but no activity and signals on idle stage."Blinking" indicates link activity on cable.
92	LNKACT4	O	8mA	**LINK/Activity LED4.** Active low"1" indicates no link activity on cable"0" indicates link okay on cable, but no activity and signals on idle stage."Blinking" indicates link activity on cable.
106	DUPCOL3	O	8mA	**Duplex/Collision LED3** Active low"1" for half-duplex and "blinking" for collision indication"0" for full-duplex indication
103	DUPCOL4	O	8mA	**Duplex/Collision LED4** Active low"1" for half-duplex and "blinking" for collision indication"0" for full-duplex indication

Table 3 LED Interface (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
107	DUPCOL2	O	8mA PU	**Duplex/Collision LED2.** Active low"1" for half-duplex and "blinking" for collision indication"0" for full-duplex indication
	SettingBPEN	O	8mA PU	**Setting BPEN** At power-on-reset, latched as Back Pressure setting "1" to enable Back-Pressure (defaulted), "0" to disable Back Pressure.At power-on-reset, latched as Back Pressure setting "1" to enable Back-Pressure (defaulted), "0" to disable Back Pressure.
108	DUPCOL1	O	8mA PD	**Duplex/Collision LED1** Active low"1" for half-duplex and "blinking" for collision indication"0" for full-duplex indication
	SettingPHYAS1	O	8mA PD	**Setting PHYAS1** Power on Reset latch value combine with TXEN. Internal pull down. Check pin 66.
109	DUPCOL0	O	8mA PU	**Duplex/Collision LED0.** Active low"1" for half-duplex and "blinking" for collision indication"0" for full-duplex indication
	SettingANEN	O	8mA PU	**Setting ANEN** On power-on-reset, latched as Auto Negotiation capability for all ports. 0_B , Disable Auto Negotiation 1_B , Enable Auto Negotiation(defaulted by pulled up internally)
50	LDSPD0	O	8mA	**Speed LED[4:0].** Used to indicate corresponding port's speed status. 0_B , 100Mb/s 1_B , 10Mb/s
51	LDSPD1	O	8mA	**Speed LED[4:0].** Used to indicate corresponding port's speed status. 0_B , 100Mb/s 1_B , 10Mb/s
54	LDSPD2	O	8mA	**Speed LED[4:0].** Used to indicate corresponding port's speed status. 0_B , 100Mb/s 1_B , 10Mb/s
55	LDSPD3	O	8mA	**Speed LED[4:0].** Used to indicate corresponding port's speed status. 0_B , 100Mb/s 1_B , 10Mb/s
58	LDSPD4	O	8mA	**Speed LED[4:0].** Used to indicate corresponding port's speed status. 0_B , 100Mb/s 1_B , 10Mb/s

2.2.4 EEPROM/Management Interface

Table 4 EEPROM/Management Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
84	EDO	I	TTL PU	**EEPROM Data Output.** Serial data input from EEPROM. This pin is internally pull-up.
80	EECS	O	4mA PD	**EEPROM Chip Select.** This pin is active high chip enable for EEPROM. When RESETL is low, it will be Tri-state. Internally Pull-down
81	EECK	I/O	4mA PD	**Serial Clock** This pin is the clock source for the EEPROM. When RESETL is low, it will be tri-state.
	SettingXOVEN	I/O	4mA PD	**Setting XOVEN** This pin is internal pull-down. On power-on-reset, latched as P4~0 Auto MDIX enable or not.“0” to disable MDIX (defaulted), “1” to enable MDIX. It is suggest this is set to external pull up to enable MDIX for all ports.
79	EDI	I/O	4mA PD	**EEPROM Serial Data Input.** This pin is the output for serial data transfer. When RESETL is low, it will be tri-state.
	SettingLEDMODE	I/O	4mA PD	**Setting LEDMODE** This pin is internal pull-down. “0” to set Single color mode for LED.“1” to set Dual Color mode for LED.

2.2.5 Power/Ground, 48 pins

Table 5 Power/Ground, 48 pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
3, 10, 16, 23, 29, 36, 42, 125	GNDA	I	-	**AD Block Ground**
6, 7, 19, 20, 32, 33, 45, 122	VCCA2	I	-	**Power Used by Tx Line Driver, 1.8 V**
13, 26, 39, 128	VCCAD	I	-	**Power Used by AD Block, 3.3 V**
119	GNDBIAS	I	-	**Bias Block Ground**
121	VCCBIAS	I	-	**Bias Block Power**
116	GNDPLL	I	-	**PLL Ground**
115	VCCPLL	I	-	**PLL Power, 1.8 V**
47, 52, 64, 76, 93, 83, 111	GNDIK	I	-	**Digital Core Ground**
48, 53, 65, 75, 82, 94, 110	VCCIK	I	-	**Digital Core Power, 1.8 V**

Table 5 Power/Ground, 48 pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
46, 57, 70, 87, 99, 104	GNDO	I	-	**Digital Pad Ground**
56, 71, 88, 105	VCC3O	I	-	**Digital Pad Power, 3.3 V**
69	GND	I	-	**Digital Pad Ground**

2.2.6 MISC

Table 6 MISC

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
85	CKO25M	O	8mA	**25M Clock Output.**
117	Control	AO	Analog	**FET Control Signal** Used to control FET for 3.3 V to 1.8 V regulator.
120	RTX	AI	Analog	**TX Resistor.** Add 1.1K%1 resister to GND.
118	VREF	AI	Analog	**Analog Reference Voltage.**
112	RC	I	SCHE	**RC Input for Power On reset** Reset input pin.
113	XI	AI	Analog	**25M Crystal Input.** Variation is limited to +/- 50ppm.
114	XO	AO	Analog	**25M Crystal Output.** When the device is connected to an oscillator, this pin should be left unconnected.
86	CFG0	I	TTL	**CFG0** Must be connected to GND.
49	TEST	I	TTL	**TEST Value.** For normal applications connect to GND.
1, 2, 4, 5, 14, 15, 17, 18, 27, 28	NC	-	-	**NC**

3 Function Description

3.1 Functional Descriptions

The ADM6996L integrates five 100Base-X physical sub-layer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, five complete 10Base-T modules, a 6 port 10/100 switch controller and one 10/100 MII/GPSI MAC and memory into a single chip for both 10Mbits/s, 100Mbits/s Ethernet switch operation. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either Full Duplex mode or Half-Duplex mode in 10Mbits/s and 100Mbits/s. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The ADM6996L consists of three major blocks:

- 10/100M PHY Block
- Switch Controller Block
- Built-in SSRAM

The interfaces used for communication between the PHY block and switch core is an MII interface.

An auto MDIX function is supported in this block. This function can be Enabled and Disabled by the hardware pin.

3.2 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair transceiver (PMD)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

3.3 100Base-X Module

The ADM6996L implements a 100Base-X compliant PCS and PMA and 100Base-TX compliant TP-PMD as illustrated in Figure 2. Bypass options for each of the major functional blocks within the 100Base-X PCS provides flexibility for various applications. 100Mbits/s PHY loop back is included for diagnostic purpose.

3.4 100Base-X Receiver

The 100Base-X receiver consists of functional blocks required to recover and condition the 125Mbits/s receive data stream. The ADM6996L implements the 100Base-X receiving state machine diagram as given in the ANSI/IEEE Standard 802.3u, Clause 24. The 125Mbits/s receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional sub-blocks:

- A/D Converter
- Adaptive Equalizer and timing recovery module
- NRZI/NRZ and serial/parallel decoder
- De-scrambler
- Symbol alignment block
- Symbol Decoder
- Collision Detect Block
- Carrier sense Block
- Stream decoder block

3.4.1 A/D Converter

A high performance A/D converter with a 125 MHz sampling rate converts signals received on the RXP/RXN pins to 6 bits data streams. It possess an auto-gain-control capability that will further improve receive performance especially under long cabling or harsh detrimental signal integrity. Due to high pass characteristic on a transformer, a built in base-line-wander correcting circuit will be cancelled out and its DC level restored.

3.4.2 Adaptive Equalizer and timing Recovery Module

All digital design is especially immune to noise environments and achieves better correlation between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates for line loss induced from twisted pairs and tracks a far end clock at 125M samples per second. Adaptive Equalizer's implemented with Feed forward and Decision Feedback techniques meet the requirement of BER with less than 10-12 for transmission on a CAT5 twisted pair cable ranging from 0 to 120 meters.

3.4.3 NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to the 4B/5B code group's boundary.

3.4.4 Data De-scrambling

The de-scrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and de-scrambled.

In order to maintain synchronization, the de-scrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the de-scrambler the hold timer starts a 722 micro second countdown. Upon detection of sufficient idle symbols within the 722 micro sec. period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given an operating network connection operating with good signal integrity. If the link state monitor does not recognize sufficient unscrambled idle symbols within the 722 micro second period, the de-scrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

3.4.5 Symbol Alignment

The symbol alignment circuit in the ADM6996L determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the de-scrambler. Once the /J/K symbol pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

3.4.6 Symbol Decoding

The symbol decoder functions is a look-up table that translates incoming 5B symbols into 4B nibbles. The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with a MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the internal RXD[3:0] signal lines where RXD[0] represents the least significant bit of the translated nibble.

3.4.7 Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are being presented on the internal RXD[3:0] synchronous receive clock, RXCLK. RXDV is asserted when the first nibble of a translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is de-asserted.

3.4.8 Receive Errors

The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

3.4.9 100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmit and receive operations until such time that a valid link is detected.

The ADM6996L performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10Mbits/s link status to form the reportable link status bit in the serial management register 1h, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 micro secs, and waits for an enable from the auto negotiation module. When received, the link-up state is entered, and the transmission and reception logic blocks become active. Should auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

3.4.10 Carrier Sense

Carrier sense (CRS) for 100Mbits/s operation is asserted upon the detection of two non contiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle symbol pair is detected in the received data stream, CRS is de-asserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

3.4.11 Bad SSD Detection

A Bad Start of Stream Delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if a carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, then the ADM6996L will assert RXER and present RXD[3:0] = 1110 to the internal MII for the cycles that correspond to received 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become de-asserted.

3.4.12 Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station’s transmitter. This station will be receiving valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all 1_B’s to a group of 84 1_B’s followed by a single 0_B. This is referred to as the FEFI idle pattern.

3.5 100Base-TX Transceiver

The ADM6996L implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmit driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetic for both the 10Base-T and the 100Base-TX transmissions with a simple RC component connection. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmission output driver selection.

3.5.1 Transmit Drivers

The ADM6996L 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range as specified in the ANSI TP-PMD standard.

3.5.2 Twisted-Pair Receiver

For 100Base-TX operation, the incoming signal is detected by the on-chip twisted-pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuits.

The ADM6996L uses an adaptive equalizer that changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

3.6 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loop back, jabber, wave shaper, and link integrity functions, as defined in the standard. Figure 3 provides an overview for the 10Base-T module.

The ADM6996L 10Base-T module is comprised of the following functional blocks:

- Manchester encoder and decoder
- Collision detector
- Link test function
- Transmit driver and receiver
- Serial and parallel interface
- Jabber and SQE test functions
- Polarity detection and correction

3.6.1 Operation Modes

The ADM6996L 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the ADM6996L functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmit and receive. In full duplex mode the ADM6996L can simultaneously transmit and receive data.

3.6.2 Manchester Encoder/Decoder

Data encoding and transmission begins when the transmission enable input (TXEN) goes high and continues as long as the transceiver is in a good link state. Transmission ends when the transmission enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a 1_B, or at the boundary of the bit cell if the last bit is 0_B.

Decoding is accomplished using a differential input receiver circuit and a phase-locked loop that separate the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more mid bit transitions are detected. Within one and a half bit times after the last bit, carrier sense is de-asserted.

3.6.3 Transmit Driver and Receiver

The ADM6996L integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmission signal are attenuated properly.

3.6.4 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential receive. The ADM6996L implements an intelligent receive squelch on the RXP/RXN differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of the packet is checked by the analog squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating the end of a packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise, causing premature end-of-packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 10 of register address 11h.

3.7 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbits/s half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbits/s full duplex and repeater mode operations, the CRS is asserted only due to receive activity.

3.8 Jabber Function

The jabber function monitors the ADM6996L output and disables the transmitter if it attempts to transmit a longer than legal sized packet. If TXEN is high for greater than 24ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be de-asserted for approximately 256 ms (the un-jab time) before the jabber function re-enables the transmit outputs. The jabber function can be disabled by programming bit 4 of register address 10h to high.

3.9 Link Test Function

A link pulse is used to check he integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.

The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100ns in duration and is transmitted every 16 ms, in the absence of transmit data.

3.10 Automatic Link Polarity Detection

The ADM6996L's 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 5 of register 10h.

3.11 Clock Synthesizer

The ADM6996L implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz +/- 50ppm

3.12 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The ADM6996L supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

Highest priority is relative to the following list:

- 100Base-TX full duplex (highest priority)
- 100Base-TX half duplex
- 10Base-T full duplex
- 10Base-T half duplex (lowest priority)

3.13 Memory Block

The ADM6996L's built in memory is divided into two blocks. One is a MAC addressing table and the other one is a data buffer.

The MAC address Learning Table size is 2048 entries with each entry occupying eight bytes length. These eight bytes of data include a 6 byte source address, VLAN information, Port information and an aging counter.

A data buffer is divided into 256 bytes/block. The ADM6996L buffer management is per port fixed block number and all ports share one global buffer. This architecture can get better memory utilization and network balance at different speeds and duplex test conditions.

Received packets will separate into several 256 bytes/block and chain together. If a packet size is more than 256 bytes then the ADM6996L will chain two or more blocks to store receiving packets.

3.14 Switch Functional Description

The ADM6996L uses a "store & forward" switching approach for the following reason:

- Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require large elastic buffers especially when bridging between a server on a 100Mbps network and clients on a 10Mbps segment.
- Store & forward switches improve overall network performance by acting as a "network cache"
- Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.15 Basic Operation

The ADM6996L receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port within the same VLAN group, where appropriate. If the destination address is not found in the address table, the ADM6996L treats the packet as a broadcast packet and forwards the packet to the other ports within the same VLAN group.

The ADM6996L automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed. If the Source Address is not found in the Address Table, the device adds it to the table.

3.15.1 Address Learning

The ADM6996L uses a hash algorithm to learn the MAC address and can learn up to 2K MAC addresses. An address is stored in the Address Table. The ADM6996L searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

1. If the SA was not found in the Address Table (a new address), the ADM6996L waits until the end of the packet (non-error packet) and updates the Address Table. If the SA was found in the Address Table, then the aging value of each corresponding entry will be reset to 0_B.
2. When the DA is PAUSE command, then the learning process will be disabled automatically by ADM6996L.

3.15.2 Address Recognition and Packet Forwarding

The ADM6996L forwards the incoming packets between bridged ports according to the Destination Address (DA) as below. All the packet forwarded will check the VLAN first. A forwarding port must be the within the same VLAN as the source port.

If the DA is a UNICAST address and the address was found in the Address Table, the ADM6996L will check the port number and act as follows:

- If the port number is equal to the port on which the packet was received, the packet is discarded.
- If the port number is different, the packet is forwarded across the bridge.
- If the DA is a UNICAST address and the address was not found, the ADM6996L treats it as a multicast packet and forwards it across the bridge.
- If the DA is a Multicast address, the packet is forwarded across the bridge.
- If the DA is a PAUSE Command (01-80-C2-00-00-01), then this packet will be dropped by the ADM6996L. The ADM6996L can issue and learn PAUSE commands.
- The ADM6996L will forward the packet with a DA of ($01\ 80\ C2\ 00\ 00\ 00_H$), filter out the packet with a DA of ($01\ 80\ C2\ 00\ 00\ 01_H$), and forward a packet with a DA of ($01\text{-}80\text{-}C2\text{-}00\text{-}00\text{-}02_H$ to $01\ 80\ C2\ 00\ 00\ 0F_H$)

3.15.3 Address Aging

Address aging is supported for topology changes such as an address moving from one port to another. When this happens, the ADM6996L internally has a 300 second timer which will “age-out” (remove) the address from the address table. The aging function can be enabled/disabled by the user. Normally, disabling an aging function is for security purposes.

3.15.4 Back off Algorithm

The ADM6996L implements the truncated exponential back off algorithm compliant to the 802.3 CSMA-CD standard. The ADM6996L will restart the back off algorithm by choosing 0-9 collision counts. The ADM6996L resets the collision counter after 16 consecutive retransmit trials.

3.15.5 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The typical number is 96 bits at a time. The value is 9.6 micro secs for 10Mbps ETHERNET, 960ns for 100Mbps fast ETHERNET and 96ns for 1000M. The ADM6996L provides an option of 92 bit gap in an EEPROM to prevent packet loss when Flow Control is turned off and clock P.P.M. values differ.

3.15.6 Illegal Frames

The ADM6996L will discard all illegal frames such as runt packets (less than 64 bytes), oversized packets (greater than 1518 or 1522 bytes) and bad CRC. Dribbling packing with good CRC value will be accepted by the ADM6996L. In case of bypass mode enable, the ADM6996L will support tag and untagged packets with sizes up to 1522 bytes. In case of non-bypass mode, the ADM6996L will support tag packets up to 1526bytes and untagged packets up to 1522bytes.

3.15.7 Half Duplex Flow Control

A back pressure function is supported for half-duplex operations. When the ADM6996L cannot allocate a receive buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision. Back Pressure is enabled by the BPEN set during RESET assertion. An Infineon proprietary algorithm is implemented inside the ADM6996L to prevent the back pressure function causing HUB partitioned under heavy traffic environment and reducing the packet loss rate to increase the whole system performance.

3.15.8 Full Duplex Flow Control

When full duplex port run out of its receive buffer, a PAUSE packet command will be issued by ADM6996L to notice the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. ADM6996L can issue or receive pause packet.

3.15.9 Broadcast Storm filter

If the Broadcast Storm filter is enabled, the broadcast packets over 50 ms of the threshold will be discarded by the threshold setting. See EEPROM Reg.10h.

Broadcast storm mode:

Time interval: 50ms

Max. packet number = 7490 in 100Base, 749 in 10Base

Table 7 The max. packet number = 7490 in 100Base, 749 in 10Base

Per Port Falling Threshold				
	00_B	01_B	10_B	11_B
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

Table 8 The max. packet number = 7490 in 100Base, 749 in 10Base

Per Port Rising Threshold				
	00_B	01_B	10_B	11_B
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

3.16 Auto TP MDIX function

At normal application which Switch connect to NIC card is by one by one TP cable. If Switch connect other device such as another Switch must by two way. First one is Cross Over TP cable. Second way is use extra RJ45 which crossover internal TX+- and RX+- signal. By second way customer can use one by one cable to connect two Switch devices. All these effort need extra cost and not good solution. ADM6996L provide Auto MDIX function which can adjust TX+- and RX+- at correct pin. User can use one by one cable between ADM6996L and other device. This function can be Enable/Disable by hardware pin and EEPROM configuration register 0x01h~0x09h bit 15. If hardware pin set all port at Auto MDIX mode then EEPROM setting is useless. If hardware pin set all port at non Auto MDIX mode then EEPROM can set each port this function enable or disable.

3.17 Port Locking

Port locking function will provide customer simple way to limit per port user number to one. If this function is turn on then ADM6996L will lock first MAC address in learning table. After this MAC address locking will never age out except Reset signal. Another MAC address which not same as locking one will be dropped. ADM6996L provide one MAC address per port. This function is per port setting. When turn on Port Locking function, recommend customer turn off aging function. See EEPROM register 0x12h bit 0~8.

3.18 VLAN setting & Tag/Untag & port-base VLAN

ADM6996L supports bypass mode and untagged port as default setting while the chip is power-on. Thus, every packet with or without tag will be forwarding to the destination port without any modification by ADM6996L. Meanwhile port-base VLAN could be enabled according to the PVID value (user define 4bits to map 16 groups written at register 13 to register 22) of the configuration content of each port.

ADM6996L also supports 16 802.1Q VLAN groups. In VLAN four bytes tag include twelve VLAN ID. ADM6996L learn user define four bits of VID. If user need to use this function, two EEPROM registers are needed to be programmed first:

* Port VID number at EEPROM register 0x01h~0x09h bit 13~10, register 28_H~$2B_H$ and register 0x2ch bit 7~0: ADM6996L will check coming packet. If coming packet is non VLAN packet then ADM6996L will use PVID as VLAN group reference. ADM6996L will use packet's VLAN value when receive tagged packet.

* VLAN Group Mapping Register. EEPROM register 013_H~022_H define VLAN grouping value. User use these register to define VLAN group.

User can define each port as Tag port or Untag port by Configuration register Bit 4. The operation of packet between Tag port and Untag port can explain by follow example:

Example1: Port receives Untag packet and send to Untag port.

ADM6996L will check the port user define four bits of VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port then this packet will forward to destination port without any change. If destination port not same VLAN as receiving port then this packet will be dropped.

Example2: Port receives Untag packet and send to Tag port.

ADM6996L will check the port user define fours bits of VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port with four byte VLAN Tag and new CRC. If destination port not same VLAN as receiving port then this packet will be dropped.

Example3: Port receives Tag packet and send to Untag port.

ADM6996L will check the packet VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port after remove four bytes with new CRC error. If destination port not same VLAN as receiving port then this packet will be dropped.

Example4: Port receives Tag packet and send to Tag port.

ADM6996L will check the user define packet VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port without any change. If destination port not same VLAN as receiving port then this packet will be dropped.

3.19 Priority Setting

It is a trend that data, voice and video will be put on networking, Switch not only deal data packet but also provide service of multimedia data. ADM6996L provides two priority queues on each port with N:1 rate. See EEPROM Reg.10_H.

This priority function can set three ways as below:

* By Port Base: Set specific port at specific queue. ADM6996L only check the port priority and not check packet's content VLAN and TOS.

* By VLAN first: ADM6996L check VLAN three priority bit first then IP TOS priority bits.

* By IP TOS first: ADM6996L check IP TOS three priority bit first then VLAN three priority bits.

If port set at VLAN/TOS priority but receiving packet without VLAN or TOS information then port base priority will be used.

3.20 LED Display

Three LED per port are provided by ADM6996L. Link/Act, Duplex/Col. & Speed are three LED display of ADM6996L. Dual color LED mode also supported by ADM6996L. For easy production purpose ADM6996L will send test signal to each LED at power on reset stage. EEPROM register 12_H define LED configuration table.

ADM6996L LED is active Low signal. Dupcol0 & Dupcol1 will check external signal at Reset time. If external signal add pull high then LED will active Low. If external signal add pull down resister then LED will drive high.

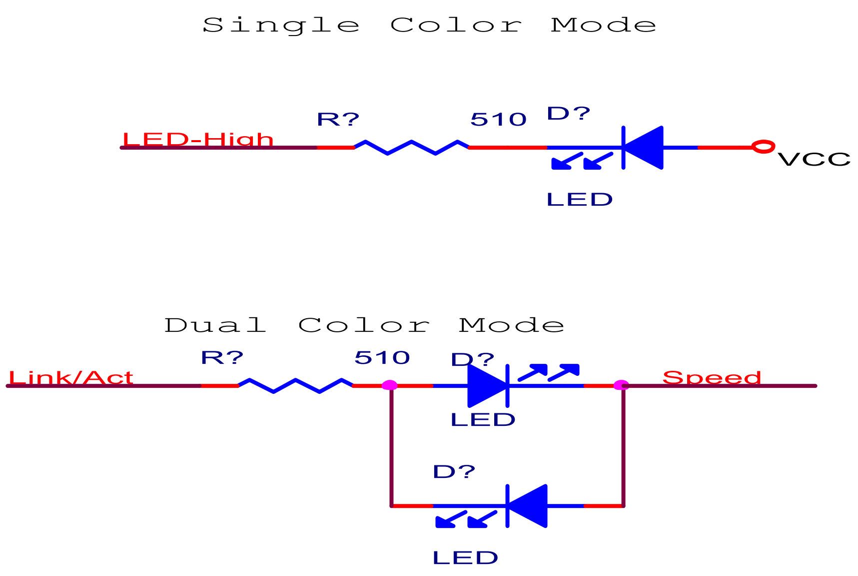

Figure 3 LED Display

4 Registers Description

4.1 EEPROM Content

Table 9 Registers Address SpaceRegisters Address Space

Module	Base Address	End Address	Note
EEPROM	00_H	33_H	

Table 10 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
SigReg	Signature Register	00_H	**27**
ConfigReg_0	Configuration Register 0	01_H	**28**
ResReg_0	Reserved Register 0	$0A_H$	**29**
ConfigReg_1	Configuration Register 1	$0B_H$	**30**
ResReg_1	Reserved Register 1	$0C_H$	**30**
ResReg_2	Reserved Register 1	$0D_H$	**30**
VLAN_Map_P	VLAN priority Map Register	$0E_H$	**31**
TOS_Priority	TOS priority Map Register	$0F_H$	**31**
ConfigReg_2	Configuration Register 2	10_H	**32**
VLAN_Mode	VLAN Mode Select Register	11_H	**33**
ConfigReg_3	Miscellaneous Configuration Register 3	12_H	**35**
VLAN_Map_T	VLAN mapping table registers	13_H	**36**
ResReg_3	Reserved Register 3	23_H	**37**
ResReg_4	Reserved Register 4	24_H	**37**
ResReg_5	Reserved Register 5	25_H	**37**
ResReg_6	Reserved Register 6	26_H	**38**
ResReg_7	Reserved Register 7	27_H	**38**
ConfigReg_4	Configuration Register 4	28_H	**38**
ConfigReg_5	Configuration Register 5	29_H	**39**
ConfigReg_6	Configuration Register 6	$2A_H$	**39**
ConfigReg_7	Configuration Register 7	$2B_H$	**40**
ConfigReg_8	Configuration Register	$2C_H$	**40**
ResReg_8	Reserved Register 8	$2D_H$	**41**
ResReg_9	Reserved Register 9	$2E_H$	**41**
PH_Restart	PHY Restart	$2F_H$	**42**
ConfigReg_	Miscellaneous Configuration Register 9	30_H	**42**
BWCon_0	Bandwidth Control Register 0	31_H	**43**
BWCon_1	Bandwidth Control Register 1	32_H	**44**
BWConEn	Bandwidth Control Enable Register	33_H	**44**

The register is addressed wordwise.

Table 11 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

Table 12 Registers Clock DomainsRegisters Clock Domains

Clock Short Name	Description

4.1.1 EEPROM Registers

Signature Register

Description

SigReg	Offset	Reset Value
Signature Register	00_H	4154_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Signature															
ro															

Field	Bits	Type	Description
Signature	15:0	ro	**Signature** 4154_H **SigReg**, Obligatory value (AT)

Note: ADM6996L will check register 0 value before read all EEPROM content. If this value not match with 0x4154h then other values in EEPROM will be useless. ADM6996L will use internal default value. User cannot write Signature register when programming ADM6996L internal register.

Configuration Register 0

Used to configure chip settings

ConfigReg_0	Offset	Reset Value
Configuration Register 0	01_H	$0040F_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAM	FSE	PV				PP		PPE	TV	PD	OT	DUP	OPS	AN	FC
rw	rw	rw				rw		rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CAM	15	rw	**Crossover Auto MDIX** 0_B **D**, Disable *Note: Hardware Reset latch value EECK can be set globally using the Auto MDIX function.* 1_B **E**, Enable
FSE	14	rw	**Fx Select Enable** 0_B **TP**, Tp Mode *Note: If this bit has been set to Fx in hardware then the bit does not have the power to change from Fx to Tp* 1_B **FX**, Fx Mode
PV	13 :10	rw	**Port VLAN ID**
PP	9:8	rw	**Port Based Priority**

Field	Bits	Type	Description
PPE	7	rw	**Port Based Priority Enable** 0_B **VTE**, VLAN or TOS Priority Enable *Note: If this bit is on only Port Bases Priority will be checked this is also the default check. If the user wants to check the VLAN priority Tag mode must be selected* 1_B **PBE**, Port Based Priority Enable
TV	6	rw	**TOS over VLAN priority** 0_B **V**, VLAN Enable 1_B **T**, TOS Enable
PD	5	rw	**Port Disable** 0_B **E**, Enable 1_B **D**, Disable
OT	4	rw	**Output Packet Tagging** 0_B **U**, Un-tag 1_B **T**, Tag
DUP	3	rw	**Duplex Enable** 0_B **H**, Half 1_B **F**, Full
OPS	2	rw	**Operating Speed** 0_B **10**, 10Mbps 1_B **100**, 100 Mbps
AN	1	rw	**Auto-negotiation** 0_B **D**, Disable 1_B **E**, Enable
FC	0	rw	**802.x Flow Control Command** 0_B **D**, Disable 1_B **E**, Enable

Reserved Register 0

Register reserved for future use

ResReg_0	Offset	Reset Value
Reserved Register 0	**$0A_H$**	**$0040F_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						**IDR**	Res								
ro						rw	ro								

Field	Bits	Type	Description
Res	15:10	ro	**Reserved**
IDR	9	rw	**Replace Packet ID** 0_B **N**, Not replaced 1_B **Y**, Replaced with 1 by PVID
Res	8:0	ro	**Reserved**

Configuration Register 1

Used to configure the chip

ConfigReg_1	Offset	Reset Value
Configuration Register 1	**$0B_H$**	**$040F_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FD	Res							**TE**	**IPG**	Res					
rw	ro							rw	rw	ro					

Field	Bits	Type	Description
FD	15	rw	**Far End Fault Detection** 0_B **D**, Disable 1_B **E**, Enable
Res	14:8	ro	**Reserved**
TE	7	rw	**Trunk Enable** 0_B **D**, Disable Port 3 and 4 1_B **E**, Enable Port 3 and 4
IPG	6	rw	**Inter Packet Gap Setting** 0_B **96B**, 96 bits 1_B **92B**, 92 bits
Res	5:0	ro	**Reserved**

Reserved Register 1

Reserved for future use

ResReg_1	Offset	Reset Value
Reserved Register 1	**$0C_H$**	**$040F_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res															
ro															

Field	Bits	Type	Description
Res	15:0	ro	**Reserved**

Reserved Register 2

Reserved for future use

ResReg_2	Offset	Reset Value
Reserved Register 1	**$0D_H$**	**$040F_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res															
ro															

Field	Bits	Type	Description
Res	15:0	ro	**Reserved**

VLAN Priority Map Register

Sets the VLAN priorities

VLAN_Map_P	**Offset**	**Reset Value**
VLAN priority Map Register	**$0E_H$**	**$040F_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
V7		**V6**		**V5**		**V4**		**V3**		**V2**		**V1**		**V0**	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
V7	15:14	rw	**Mapped priority of tag value (VLAN)**
V6	13:12	rw	
V5	11:10	rw	
V4	9:8	rw	
V3	7:6	rw	
V2	5:4	rw	
V1	3:2	rw	
V0	1:0	rw	

Note: Value 3 ~ 0 are for priority queue Q3~Q0 respectively.The Weight ratio is Q3: Q2: Q1: Q0 = 8: 4: 2: 1. The default is port-base priority for un-tagged packets and non_IP frame.

Type of Service (TOS) Priority Map Register

Sets TOS priority

TOS_Priority	**Offset**	**Reset Value**
TOS priority Map Register	**$0F_H$**	**5500_H**

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
T7	**T6**	**T5**	**T4**	**T3**	**T2**	**T1**	**T0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
T7	15:14	rw	**Mapped priority of tag value (TOS)**
T6	13:12	rw	
T5	11:10	rw	
T4	9:8	rw	
T3	7:6	rw	
T2	5:4	rw	
T1	3:2	rw	
T0	1:0	rw	

Note: Value 3 ~ 0 are for priority queues Q3~Q0 respectively. The Weight ratio is Q3: Q2: Q1: Q0 = 8: 4: 2: 1. The default is port-based priority for un-tagged packets and non_IP frames.

Table 13 Ethernet Packet from Layer 2

Preamble/SFD	Destination (6 bytes)	Source (6 bytes)	Packet length (2 bytes)	Data (46-1500 bytes)	CRC (4 bytes)
	Byte 0~5	Byte 6~11	Byte 12~13	Byte 14~	

Configuration Register 2

Used to configure the chip

ConfigReg_2	Offset	Reset Value
Configuration Register 2	10_H	0040_H

15 14	13 12	11 10	9 8	7	6	5	4	3	2	1 0
Q3	**Q2**	**Q1**	**Q0**	**AGE**	Res	Res	**XC**	Res	**SF**	**ST**
rw	rw	rw	rw	rw	ro	ro	rw	rw	rw	rw

Field	Bits	Type	Description
Q3	15:14	rw	**Discard mode** Drop scheme for Queue n
Q2	13:12	rw	
Q1	11:10	rw	
Q0	9:8	rw	
AGE	7	rw	**Aging Status** 0_B **E**, Enable 1_B **D**, Disable

Field	Bits	Type	Description
Res	6	ro	**Reserved**
Res	5	ro	**Reserved**
XC	4	rw	**CRC Check** 0_B **E**, Enable CRC check 1_B **D**, Disable CRC check
Res	3	rw	**Reserved**
SF	2	rw	**Broadcast Storm Filter** 0_B **D**, Disable 1_B **E**, Enable
ST	1:0	rw	**Broadcast Storm Threshold** See below Table 5 and Table 6 for details on the Broadcast Storm Threshold

Note: Broadcast storm initial time interval = 50ms. The max. packet number = 7490 in 100Base, 749 in 10Base

Table 14 Per Port Rising Threshold

	00	01	10	11
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

Table 15 Per Port Falling Threshold

	00	01	10	11
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

Table 16 Drop Scheme for Each Queue

Discard Mode Utilization	00	01	10	11
TBD	0%	0%	25%	50%

VLAN mode select Register

Selects VLAN Mode

VLAN_Mode VLAN Mode Select Register	Offset 11_H	Reset Value $FF00_H$

15–8	7–6	5	4	3–0
Res	Res	**VM**	**MAC**	Res
ro	ro	rw	rw	ro

Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
Res	7:6	ro	**Reserved**
VM	5	rw	**VLAN Mode Select** 0_B **P**, Port based by-pass mode 1_B **Q**, 802.1Q based
MAC	4	rw	**MAC Clone Enable** 0_B **N**, Normal Mode.Learning with SA only. The MAC table will be searched or filled using only SA or DA. 1_B **M**, Mac Mode. Learned using SA VID0. MAC table will be searched or filled using VID0 SA or DA. This bit allows two identical addresses with different VID0 to be learned.
Res	3:0	ro	**Reserved**

Note:

Below is an example of a VLAN Tag and a MAC application for Bit4 and Bit5.

Below is an old router architecture example. The disadvantages of this are:

1. WAN port only supports 10M Half-Duplex and non-MDIX functions
2. Needs extra 10M NIC cost.
3. ISA bus will become a bottleneck for the whole system

Below is new architecture by using ADM6996L serial chip VLAN function. The advantages of below are:

- WAN Port can upgrade to 100/10 Full/Half, Auto MDIX.
- WAN/LAN Port is programmable and put on same Switch.
- No need extra NIC and save lot of cost.
- High bandwidth of MII port up to 200M speed.

New Router application works well on normal application. If user's ISP vendor(cable modem) lock Registration Card's ID then Router CPU must send this Lock Registration Card's ID to WAN Port. One condition happen is there exist two same MAC ID on this Switch. One is original Card and another one is CPU. This will make Switch learning table trouble.

ADM6996L provide MAC Clone function that allow two same MAC address with different VLAN ID0 on learning table. This will solve Lock registration Card's ID issue. AT8989P serial chip will put these two same MAC addresses with different VLAN ID0 at different learning table entry.

How to Set ADM6996L on Router.

Port0~3: LAN Port.

Port4: WAN Port.

Port5: MII Port as CPU Port.

Step1: Set Register 11_H bit4 and bit5 to 1.

{Coding: Write Register 11_H as $FF30_H$}

Step2: Set Port0~3 as Untag Port and set PVID=1.

{Coding: Write Register 01_H, 03_H, 05_H, 07_H as $840F_H$. Port0~3 as Untag, PVID=1, Enable MDIX}

Step3: Set Port4 as Untag Port and set PVID=2.

{Coding:Write Register 08_H as $880F_H$. Port4 as Untag, PVID=2, Enable MDIX.}

Step4: Set Port5 MII Port as Tag Port and set PVID=2.
{Coding:Write Register 09_H as $881F_H$. Port5 MII port as Tag, PVID=2.}
Step5: Group Port0, 1, 2, 3, 5 as VLAN 1.
{Coding: Write Register 14_H as 0155_H. VLAN1 cover Port0, 1, 2, 3, 5.}
Step6: Group Port4, 5 as VLAN 2.
{Coding: Write Register 15_H as 0180_H. VLAN2 cover Port4, 5.}

How MAC Clone Operation:

- LAN to LAN/CPU Traffic.

ADM6996L LAN traffic to LAN/CPU only. Traffic to another LAN port will be untag packet. Traffic to CPU is Tag packet with VID=1. CPU can check VID to distinguish LAN traffic or WAN traffic.

- WAN to CPU Traffic.

ADM6996L WAN traffic to CPU only. Traffic to CPU is Tag packet with VID=2. CPU can check VID to distinguish LAN traffic or WAN traffic.

- CPU to LAN Packet.

ADM6996L CPU Packet to LAN port must add VID=1 in VLAN field.
ADM6996L check VID to distinguish LAN traffic or WAN traffic. LAN output packet is Untag.

- CPU to WAN Packet.

ADM6996L CPU Packet to WAN port must add VID=2 in VLAN filed.
ADM6996L check VID to distinguish LAN traffic or WAN traffic. WAN output packet is Untag.

- ADM6996L learning sequence

ADM6996L will check VLAN mapping setting first then check learning table.
User does not worry LAN/WAN traffic mix up.
Bit 10: Half Duplex Back Pressure enable. 1/enable, 0/disable.

Configuration Register 3

ConfigReg_3	**Offset**	**Reset Value**
Miscellaneous Configuration Register 3	**12_H**	**3600_H**

15	14	13–12	11	10–9	8	7	6	5	4	3	2	1	0
CD	Res	Res	Res	Res	**ML5**	**ML4**	**ML3**	Res	**ML2**	Res	**ML1**	Res	**ML0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CD	15	rw	**Excessive Collision Drop** 0_B **D**, Disable 1_B **E**, Enable

Field	Bits	Type	Description
Res	14	rw	**Reserved**
Res	13:12	rw	**Reserved**
Res	11	rw	**Reserved**
Res	10:9	rw	**Reserved**
ML5	8	rw	**Port5 MAC Lock** 0_B **D**, Disable 1_B **LM**, Lock first MAC Source Address
ML4	7	rw	**Port4 MAC Lock** 0_B **D**, Disable 1_B **LM**, Lock first MAC Source Address
ML3	6	rw	**Port3 MAC Lock** 0_B **D**, Disable 1_B **LM**, Lock first MAC Source Address
Res	5	rw	**Reserved**
ML2	4	rw	**Port 2 MAC Lock** 0_B **D**, Disable 1_B **LM**, Lock first MAC source address
Res	3	rw	**Reserved**
ML1	2	rw	**Port1 MAC Lock** 0_B **D**, Disable 1_B **LM**, Lock first MAC source address
Res	1	rw	**Reserved**
ML0	0	rw	**Port0 MAC Lock** 0_B **D**, Disable 1_B **LM**, Lock first MAC source address

VLAN Mapping Table Registers

VLAN_Map_T — **Offset** — **Reset Value**
VLAN mapping table registers — **13_H** — **$FFFF_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res							**VM5**	**VM4**	**VM3**	Res	**VM2**	Res	**VM1**	Res	**VM0**
ro							rw	rw	rw	ro	rw	ro	rw	ro	rw

Field	Bits	Type	Description
Res	15:9	ro	**Reserved**
VM5	8	rw	**Port 5 VLAN Mapping**
VM4	7	rw	**Port 4 VLAN Mapping**
VM3	6	rw	**Port 3 VLAN Mapping**
Res	5	ro	**Reserved**

Field	Bits	Type	Description
VM2	4	rw	**Port 2 VLAN Mapping**
Res	3	ro	**Reserved**
VM1	2	rw	**Port 1 VLAN Mapping**
Res	1	ro	**Reserved**
VM0	0	rw	**Port 0 VLAN Mapping**

Note: 16 VLAN Group: See Register $2C_H$ bit 11. Select the VLAN group ports and set the corresponding bits to 1.

Reserved Register 3

ResReg_3	Offset	Reset Value
Reserved Register 3	**23_H**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res															
rw															

Field	Bits	Type	Description
Res	15:0	rw	**Reserved**

Reserved Register 4

ResReg_4	Offset	Reset Value
Reserved Register 4	**24_H**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res															
rw															

Field	Bits	Type	Description
Res	15:0	rw	**Reserved**

Reserved Register 5

ResReg_5	Offset	Reset Value
Reserved Register 5	**25_H**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res															
rw															

Field	Bits	Type	Description
Res	15:0	rw	**Reserved**

Reserved Register 6

ResReg_6 **Offset** **Reset Value**
Reserved Register 6 **26_H** **0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res															
rw															

Field	Bits	Type	Description
Res	15:0	rw	**Reserved**

Reserved Register 7

ResReg_7 **Offset** **Reset Value**
Reserved Register 7 **27_H** **0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res															
rw															

Field	Bits	Type	Description
Res	15:0	rw	**Reserved**

Configuration Register 4

ConfigReg_4 **Offset** **Reset Value**
Configuration Register 4 **28_H** **0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res								**P0**							
ro								rw							

Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
P0	7:0	rw	**Port 0 PVID** 0001_H **PVID**, These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Configuration Register 5

ConfigReg_5	**Offset**	**Reset Value**
Configuration Register 5	**29_H**	**$0000\ 0000_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res								**P1**							
ro								rw							

Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
P1	7:0	rw	**Port1 PVID bit 11~4.** 0003_H **PVID 1**, These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Configuration Register 6

ConfigReg_6	**Offset**	**Reset Value**
Configuration Register 6	**$2A_H$**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res								**P2**							
ro								rw							

Field	Bits	Type	Description
Res	15:8	ro	**Reserved**

Field	Bits	Type	Description
P2	7:0	rw	**Port2 PVID bit 11~4.** 0005_H **PVID 2**, These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Configuration Register 7

ConfigReg_7	Offset	Reset Value
Configuration Register 7	$2B_H$	0000_H

15–8	7–0
P4	P3
ro	rw

Field	Bits	Type	Description
P4	15:8	ro	**Port4 PVID bit 11~4.** 0008_H **PVID 1**, These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.
P3	7:0	rw	**Port3 PVID bit 11~4.** 0007_H **PVID 1**, These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Configuration Register 8

ConfigReg_8	Offset	Reset Value
Configuration Register	$2C_H$	$D000_H$

15	14	13	12	11	10–8	7–0
CR0	CR1	CR2	CR3	Res	VS	P5
rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CR0	15	rw	**Control Reserved MAC** Control reserved MAC (0180C2000000) 0_B **D**, Discard 1_B **F**, Forward
CR1	14	rw	**Control Reserved MAC** Control reserved MAC (0180C2000001) 0_B **D**, Discard 1_B **F**, Forward

Field	Bits	Type	Description
CR2	13	rw	**Control Reserved MAC** Control reserved MAC (0180C2000002- 0180C200000F) 0_B **D**, Discard 1_B **F**, Forward
CR3	12	rw	**Control Reserved MAC** Control reserved MAC (0180C2000010-0180C20000FF) 0_B **D**, Discard 1_B **F**, Forward
Res	11	rw	**Reserved**
VS	10:8	rw	**VLAN Grouping Tag Shift** 0_D **VID0**, VID [3:0] 1_D **VID1**, VID [4:1] 2_D **VID2**, VID [5:2] 3_D **VID3**, VID [6:3] 4_D **VID4**, VID [7:4] 5_D **VID5**, VID [8:5] 6_D **VID6**, VID [9:6] 7_D **VID7**, VID [10:7]
P5	7:0	rw	**Port5 PVID bit 11~4.** 0009_H **PVID 1**, These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Note: Bit[10:8]: VLAN Tag shift register. ADM6996L will select 4 bit form total 12 bit VID as VLAN group reference.
Bit[15:12]: IEEE 802.3 reserved DA forward or drop police.

Reserved Register 8

ResReg_8	Offset	Reset Value
Reserved Register 8	**$2D_H$**	**4442_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res															
rw															

Field	Bits	Type	Description
Res	15:0	rw	**Reserved**

Reserved Register 9

ResReg_9	Offset	Reset Value
Reserved Register 9	**$2E_H$**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res															
rw															

Field	Bits	Type	Description
Res	15:0	rw	**Reserved**

PHY Restart

PH_Restart **Offset** **Reset Value**
PHY Restart **2F$_H$** **0000$_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PR															
rw															

Field	Bits	Type	Description
PR	15:0	rw	**PHY Restart** 0000$_H$ **PHY Restart**, Writing this Hex value to this register restarts the internal PHYs.

Configuration Register 9

ConfigReg_ **Offset** **Reset Value**
Miscellaneous Configuration Register 9 **30$_H$** **0987$_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			**LM**	Res	Res	**LC**	Res	Res	**RCL**	**MAC**	Res				
rw			rw	rw	rw	rw	rw	rw	rw	rw	rw				

Field	Bits	Type	Description
Res	15:13	rw	**Reserved**
LM	12	rw	**Port 4 LED Mode** 0$_B$ **D**, LinkAct/DupCol/Speed 1$_B$ **S**, LinkAct/Speed
Res	11	rw	**Reserved**
Res	10	rw	**Reserved**

Field	Bits	Type	Description
LC	9	rw	**Color LED** 0_B **N**, Normal LED Port1 Col LED, 100M Col LED. 1_B **D**, Dual Speed Hub LEDPort0 Color LED, 10M Color LED.
Res	8	rw	**Reserved**
Res	7	rw	**Reserved**
RCL	6	rw	**MII Speed Double** 0_B **25**, TxCLK max speed is 25 MHz 1_B **50**, TxCLK max speed is 50 MHz
MAC	5	rw	**Mac Clone Enable** MAC Clone Enable Bit[1].
Res	4:0	rw	**Reserved**

Bandwidth Control Register

BWCon_0	**Offset**	**Reset Value**
Bandwidth Control Register 0	31_H	0000_H

31–16	15	14:12	11	10:8	7	6:4	3	2:0
Res	**RC 3**	**P3T**	**RC 2**	**P2T**	**RC 1**	**P1T**	**RC 0**	**P0T**
	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RC3	15	rw	**Receive Packet Length Count** Counted on the Source Port 3. 0_D **R3**, The switch will add length to the P3 counter
P3T	14:12	rw	**Port 3 Threshold Control Meter** Reference table in note below.
RC2	11	rw	**Receive Packet Length Count** Counted on the Source Port 2. 0_D **R2**, The switch will add length to the P2 counter
P2T	10:8	rw	**Port 2 Threshold Control Meter** Reference table in note below.
RC1	7	rw	**Receive Packet Length Count** Counted on the Source Port 1. 0_D **R1**, The switch will add length to the P1 counter
P1T	6:4	rw	**Port 1 Threshold Control Meter** Reference table in note below.
RC0	3	rw	**Receive Packet Length Count** Counted on the Source Port 0. 0_D **R0**, The switch will add length to the P2 counter
P0T	2:0	rw	**Port 0 Threshold Control Meter** Reference table in note below.

Table 17 Note:Reference Table

000	001	010	011	100	101	110	111
256K	512K	1M	2M	5M	10M	20M	50M

Bandwidth Control Register 1

BWCon_1	**Offset**	**Reset Value**
Bandwidth Control Register 1	**32_H**	**0000_H**

15:8	7	6:4	3	2:0
Res	**RC5**	**P5T**	**RC4**	**P4T**
ro	rw	rw	rw	rw

Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
RC5	7	rw	**Receive Packet Length Count** Counted on the Source Port 5. 0_D **Count5**, The switch will add length to the P5 counter
P5T	6:4	rw	**Port 5 Threshold Control Meter** Reference table in note below.
RC4	3	rw	**Receive Packet Length Count** Counted on the Source Port 4. 0_D **Count4**, The switch will add length to the P4 counter
P4T	2:0	rw	**Port 4 Threshold Control Meter** Reference table in note below.

Table 18 Note:Reference Table

000	001	010	011	100	101	110	111
256K	512K	1M	2M	5M	10M	20M	50M

Bandwidth Control Enable Register

BWConEn	**Offset**	**Reset Value**
Bandwidth Control Enable Register	**33_H**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res							**BW5**	**BW4**	**BW3**	Res	**BW2**	Res	**BW1**	Res	**BW0**
ro							rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Res	15:9	ro	**Reserved**
BW5	8	rw	**Port 5 Bandwidth Control Enable** 0_B **D**, Disable 1_B **E**, Enable
BW4	7	rw	**Port 4 Bandwidth Control Enable** 0_B **D**, Disable 1_B **E**, Enable
BW3	6	rw	**Port 3 Bandwidth Control Enable** 0_B **D**, Disable 1_B **E**, Enable
Res	5	rw	**Reserved**
BW2	4	rw	**Port 2 Bandwidth Control Enable** 0_B **D**, Disable 1_B **E**, Enable
Res	3	rw	**Reserved**
BW1	2	rw	**Port 1 Bandwidth Control Enable** 0_B **D**, Disable 1_B **E**, Enable
Res	1	rw	**Reserved**
BW0	0	rw	**Port 0 Bandwidth Control Enable** 0_B **D**, Disable 1_B **E**, Enable

4.2 Serial Register Map

Table 19 Registers Address SpaceRegisters Address Space

Module	Base Address	End Address	Note
Serial	00_H	$3C_H$	

Table 20 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
ChipID	Chip Identifier Register	00_H	**47**
PortStat_0	Port Status Register 0	01_H	**47**
PortStat_1	Port Status Register 1	02_H	**49**
CabStat	Cable Broken Status	03_H	**50**
OverFlow_0	Over Flow Flag 0 Register 0	$3A_H$	**50**
OverFlow_1	Over Flow Flag 0 Register 1	$3B_H$	**51**
OverFlow_2	Over Flow Flag 2 Register	$3C_H$	**52**

The register is addressed wordwise.

Table 21 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared

Table 21 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

Table 22 Registers Clock DomainsRegisters Clock Domains

Clock Short Name	Description

4.2.1 Serial Registers

Chip Identifier Register

ChipID **Chip Identifier Register**	**Offset** **00$_H$**	**Reset Value** **0000 0000$_H$**

31 … 4	3 … 0
ID	**Ver**
ro	ro

Field	Bits	Type	Description
ID	31:4	ro	**Chip Identifier Register** 0000 7101$_H$ **ID**, Chip Identifier
Ver	3:0	ro	**Version No** 0000$_H$ **Ver**, Version No.

Port Status Register 0

PortStat_0 **Port Status Register 0**	**Offset** **01$_H$**	**Reset Value** **0000 0000$_H$**

31	30	29	28	27	26	25	24	23 22 21 20	19	18	17	16	15 14 13 12	11	10	9	8	7 6 5 4	3	2	1	0
FP 4	DP 4	SP 4	LP 4	FP 3	DP 3	SP 3	LP 3	Res	FP 2	DP 2	SP 2	LP 2	Res	FP 1	DP 1	SP 1	LP 1	Res	FP 0	DP 0	SP 0	LP 0
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
FP4	31	ro	**Port 4 Flow Control Enable** 0_B **D**, Flow Control Disable 1_B **FC4**, 802.3X on for full duplex or back pressure on for half duplex.
DP4	30	ro	**Port 4 Duplex Status** 0_B **H**, Half Duplex 1_B **F**, Full Duplex
SP4	29	ro	**Port 4 Speed Status** 0_B **10**, 10Mbps 1_B **100**, 100Mbps
LP4	28	ro	**Port 4 Linkup Status** 0_B **NE**, Link is not established. 1_B **E**, Link is established.
FP3	27	ro	**Port 3 Flow Control Enable** 0_B **D**, Flow Control Disable 1_B **FC3**, 802.3X on for full duplex or back pressure on for half duplex.
DP3	26	ro	**Port 3 Duplex Status** 0_B **H**, Half Duplex 1_B **F**, Full Duplex
SP3	25	ro	**Port 3 Speed Status** 0_B **10**, 10Mbps 1_B **100**, 100Mbps
LP3	24	ro	**Port 3 Linkup Status** Port 3 Linkup Status: 0_B **N**, Link is not established. 1_B **E**, Link is established.
Res	23:20	ro	**Reserved**
FP2	19	ro	**Port 2 Flow Control Enable** 0_B **D**, Flow Control Disable 1_B **FC2**, 802.3X on for full duplex or back pressure on for half duplex.
DP2	18	ro	**Port 2 Duplex Status** 0_B **H**, Half Duplex 1_B **F**, Full Duplex
SP2	17	ro	**Port 2 Speed Status** 0_B **10**, 10Mbps 1_B **100**, 100Mbps
LP2	16	ro	**Port 2 Linkup Status** Port 2 Linkup Status: 0_B **NE**, Link is not established. 1_B **E**, Link is established.
Res	15:12	ro	**Reserved**

Field	Bits	Type	Description
FP1	11	ro	**Port 1 Flow Control Enable** 0_B **D**, Flow Control Disable 1_B **FC1**, 802.3X on for full duplex or back pressure on for half duplex.
DP1	10	ro	**Port 1 Duplex Status** 0_B **H**, Half Duplex 1_B **F**, Full Duplex
SP1	9	ro	**Port 1 Speed Status** 0_B **10**, 10Mbps 1_B **100**, 100Mbps
LP1	8	ro	**Port 1 Linkup Status** 0_B **NE**, Not established. 1_B **E**, Established.
Res	7:4	ro	**Reserved**
FP0	3	ro	**Port 0 Flow Control Enable** 0_B **D**, Flow Control Disable 1_B **FC0**, 802.3X on for full duplex or back pressure on for half duplex.
DP0	2	ro	**Port 0 Duplex Status** 0_B **H**, Half Duplex 1_B **F**, Full Duplex
SP0	1	ro	**Port 0 Speed Status** 0_B **10**, 10Mbps 1_B **100**, 100Mbps
LP0	0	ro	**Port 0 Linkup Status** 0_B **NE**, Not established. 1_B **E**, Established.

Port Status Register 1

PortStat_1	**Offset**	**Reset Value**
Port Status Register 1	**02_H**	**$0000\ 0000_H$**

31–5	4	3	2–1	0
Res	FP5	DP5	SP5	LP5
ro	ro	ro	ro	ro

Field	Bits	Type	Description
Res	31:5	ro	**Reserved**
FP5	4	ro	**Port 5 Flow Control Enable** 0_B **D**, Flow Control Disable 1_B **FC5**, 802.3X on for full duplex or back pressure on for half duplex.
DP5	3	ro	**Port 5 Duplex Status** 0_B **H**, Half Duplex 1_B **F**, Full Duplex

Field	Bits	Type	Description
SP5	2:1	ro	**Port 5 Speed Status** 0_B **10**, 10Mbps 1_B **100**, 100Mbps
LP5	0	ro	**Port 5 Linkup Status** 0_B **NE**, Not established. 1_B **E**, Established.

Cable Broken Status Register

CabStat	**Offset**	**Reset Value**
Cable Broken Status	**03_H**	**$0000\ 0000_H$**

31–24	23	22–21	20	19–18	17–15	14	13–12	11–9	8	7–6	5–3	2	1–0
Res	CB4	CL4	CB3	CL3	Res	CB2	CL2	Res	CB1	CL1	Res	CB0	CL0
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
Res	31:24	ro	**Reserved**
CB4	23	ro	**Port 4 Cable Broken**
CL4	22:21	ro	**Port 4 Cable Broken Length**
CB3	20	ro	**Port 3 Cable Broken**
CL3	19:18	ro	**Port 3 Cable Broken Length**
Res	17:15	ro	**Reserved**
CB2	14	ro	**Port 2 Cable Broken**
CL2	13:12	ro	**Port 2 Cable Broken Length**
Res	11:9	ro	**Reserved**
CB1	8	ro	**Port 1 Cable Broken**
CL1	7:6	ro	**Port 1 Cable Broken Length**
Res	5:3	ro	**Reserved**
CB0	2	ro	**Port 0 Cable Broken**
CL0	1:0	ro	**Port 0 Cable Broken Length**

Over Flow Flag 0 Register 0

OverFlow_0	**Offset**	**Reset Value**
Over Flow Flag 0 Register 0	**$3A_H$**	**$0000\ 0000_H$**

31–18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	OR5	OR4	OR3	Res	OR2	Res	OR1	Res	OR0	OF5	OF4	OF3	Res	OF2	Res	OF1	Res	OF0
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
Res	31:18	ro	**Reserved**
OR5	17	ro	**Overflow of Port 5 Receive Packet Byte Count**
OR4	16	ro	**Overflow of Port 4 Receive Packet Byte Count**
OR3	15	ro	**Overflow of Port 3 Receive Packet Byte Count**
Res	14	ro	**Reserved**
OR2	13	ro	**Overflow of Port 2 Receive Packet Byte Count**
Res	12	ro	**Reserved**
OR1	11	ro	**Overflow of Port 1 Receive Packet Byte Count**
Res	10	ro	**Reserved**
OR0	9	ro	**Overflow of Port 0 Receive Packet Byte Count**
OF5	8	ro	**Overflow of Port 5 Receive Packet Count**
OF4	7	ro	**Overflow of Port 4 Receive Packet Count**
OF3	6	ro	**Overflow of Port 3 Receive Packet Count**
Res	5	ro	**Reserved**
OF2	4	ro	**Overflow of Port 2 Receive Packet Count**
Res	3	ro	**Reserved**
OF1	2	ro	**Overflow of Port 1 Receive Packet Count**
Res	1	ro	**Reserved**
OF0	0	ro	**Overflow of Port 0 Receive Packet Count**

Over Flow Flag 0 Register 1

OverFlow_1	**Offset**	**Reset Value**
Over Flow Flag 0 Register 1	**$3B_H$**	**$0000\ 0000_H$**

31–18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	OB5	OB4	OB3	Res	OB2	Res	OB1	Res	OB0	OF5	OF4	OF3	Res	OF2	Res	OF1	Res	OF0
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
Res	31:18	ro	**Reserved**
OB5	17	ro	**Overflow of Port 5 Transmit Packet Byte Count**
OB4	16	ro	**Overflow of Port 4 Transmit Packet Byte Count**
OB3	15	ro	**Overflow of Port 3 Transmit Packet Byte Count**

Field	Bits	Type	Description
Res	14	ro	**Reserved**
OB2	13	ro	**Overflow of Port 2 Transmit Packet Byte Count**
Res	12	ro	**Reserved**
OB1	11	ro	**Overflow of Port 1 Transmit Packet Byte Count**
Res	10	ro	**Reserved**
OB0	9	ro	**Overflow of Port 0 Transmit Packet Byte Count**
OF5	8	ro	**Overflow of Port 5 Transmit Packet Count**
OF4	7	ro	**Overflow of Port 4 Transmit Packet Count**
OF3	6	ro	**Overflow of Port 3 Transmit Packet Count**
Res	5	ro	**Reserved**
OF2	4	ro	**Overflow of Port 2 Transmit Packet Count**
Res	3	ro	**Reserved**
OF1	2	ro	**Overflow of Port 1 Transmit Packet Count**
Res	1	ro	**Reserved**
OF0	0	ro	**Overflow of Port 0 Transmit Packet Count**

Over Flow Flag 2 Register

OverFlow_2	**Offset**	**Reset Value**
Over Flow Flag 2 Register	**$3C_H$**	**$0000\ 0000_H$**

31:18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	OE5	OE4	OE3	Res	OE2	Res	OE1	Res	OE0	OF5	OF4	OF3	Res	OF2	Res	OF1	Res	OF0
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
Res	31:18	ro	**Reserved**
OE5	17	ro	**Overflow of Port 5 Error Count**
OE4	16	ro	**Overflow of Port 4 Error Count**
OE3	15	ro	**Overflow of Port 3 Error Count**
Res	14	ro	**Reserved**
OE2	13	ro	**Overflow of Port 2 Error Count**
Res	12	ro	**Reserved**
OE1	11	ro	**Overflow of Port 1 Error Count**
Res	10	ro	**Reserved**
OE0	9	ro	**Overflow of Port 0 Error Count**
OF5	8	ro	**Overflow of Port 5 Collision Count**
OF4	7	ro	**Overflow of Port 4Collision Count**
OF3	6	ro	**Overflow of Port 3Collision Count**
Res	5	ro	**Reserved**

Field	Bits	Type	Description
OF2	4	ro	**Overflow of Port 2 Collision Count**
Res	3	ro	**Reserved**
OF1	2	ro	**Overflow of Port 1 Collision Count**
Res	1	ro	**Reserved**
OF0	0	ro	**Overflow of Port 0 Collision Count**

4.3 VLAN Packet

Table 23 VLAN Packet

Tag Protocol TD 8100	Tag Control Information TCI	LEN Length	Routing Information
Byte 12~13	Byte14~15	Byte 16~17	Byte 18

Note: ADM6996L will check packet byte 12 &13. If byte[12:13]=8100h then this packet is a VLAN packet

Byte 14~15: Tag Control Information TCI

Bit[15:13]: User Priority 7~0

Bit 12: Canonical Format Indicator (CFI)

Bit[11~0]: VLAN ID. The ADM6996L will use bit[3:0] as VLAN group.

4.4 TOS IP Packet

Table 24 TOS IP Packet

Type 0800	IP Header
Byte 12~13	Byte 14~15

Note: ADM6996L checks bytes 12 &13. If this value is 0800_H then the ADM6996L knows this is a TOP priority packet.

IP header define

Byte 14

Bit[7:0]: IP protocol version number & header length.

Byte 15: Service type

Bit[7~5]: IP Priority (Precedence) from 7~0

Bit 4: No Delay (D)

Bit 3: High Throughput

Bit 2: High Reliability (R)

Bit[1:0]: Reserved

4.5 EEPROM Access

Customer can select ADM6996L read EEPROM contents as chip setting or not. ADM6996L will check the signature of EEPROM to decide read content of EEPROM or not.

Table 25 RESETL & EEPROM content relationship

RESETL	CS	SK	DI	DO
0	High Impedance	High Impedance	High Impedance	High Impedance
Rising edge 01 (30ms)	Output	Output	Output	Input
1 (after 30ms)	Input	Input	Output	Input

Keep at least 30ms after RESETL from 01. ADM6996L will read data from EEPROM. After RESETL if CPU update EEPROM that ADM6996L will update configuration registers too.

When CPU programming EEPROM & ADM6996L, ADM6996L recognizes the EEPROM WRITE instruction only. If there is any Protection instruction before or after the EEPROM WRITE instruction, CPU needs to generate separated CS signal cycle for each Protection & WRITE instruction.

CPU can directly program ADM6996L after 30ms of Reset signal rising edge with or without EEPROM

ADM6996L serial chips will latch hardware-reset value as recommend value. It includes EEPROM interface:

EECS: Internal Pull down 40K resister.

EESK: TP port Auto-MDIX select. Internal pull down 40K resister as non Auto-MDIX mode.

EDI: Dual Color Select. Internal pull down 40K resister as Single Color Mode.

EDO: EEPROM enable. Internal pull up 40K resister as EEPROM enable.

Below Figure is ADM6996L serial chips EEPROM pins operation at different stage. Reset signal is control by CPU with at least 100ms low. Point1 is Reset rising edge. CPU must prepare proper value on EECS(0), EESK, EDI, EDO(1) before this rising edge. ADM6996L will read this value into chip at Point2. CPU must keep these values over point2. Point2 is 200ns after Reset rising edge.

ADM6996L serial chips will read EEPROM content at Point4 which 800ns far away from the rising edge of Reset. CPU must turn EEPROM pins EECS, EESK, EDI and EDO to High-Z or pull high before Point4.

If user want change state to High-Z or pull high on EEPROM pins, the order is CS-> DI -> DO -> SK is better.

A little bit different with the timing on writing EEPROM. See below graph. Must be carefully is when CS go down after write a command, SK must issue at least one clock. This is a difference between ADM6996L with EEPROM write timing. If system without EEPROM then user must write ADM6996L internal register by 93C66 timing. If user uses EEPROM then the writing timing is depend on EEPROM type.

4.6 Serial Interface Timing

ADM6996L serial chip's internal counter or EEPROM access timing

EESK: Similar to the MDC signal.

EDI: Similar to the MDIO signal

ECS: Must keep be kept low.

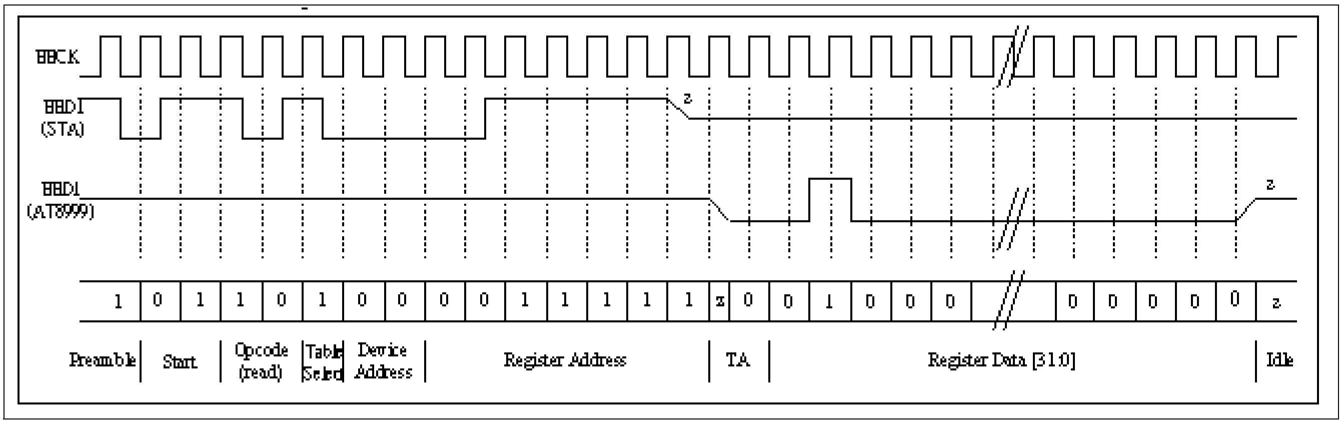

Figure 4 ADM6996L Serial Chip's Internal Counter or EEPROM Access Timing

Preamble: At least 32 continuous 1_B's

Start: 01_B(2 bits)

Opcode: 10_B (2 bits, Only supports a read command)

Table select: 1_B = Counter, 0_B = EEPROM (1 bit)

Register Address: Read Target register address. (7 bits)

TA: Turn Around.

Register Data: 32 bit data.

Counter output bit sequence is bit 31 to bit 0.

If a user reads the EEPROM then 32 bits of data will separate as two EEPROM registers. The sequence is:

1. Register +1, Register (Register is even number)
2. Register, Register-1(Register is Odd number)

Example:

Read Register 00_H then the ADM6996L will drive 01_H & 00_H

Read Register 03_H then ADM6996L will drive 03_H & 02_H

Idle: EESK must send at least one clock pulse at idle time

ADM6996L issue Reset internal counter command

EESK: Similar to the MDC signal

EDI: Similar to the MDIO signal

ECS: Must keep low.

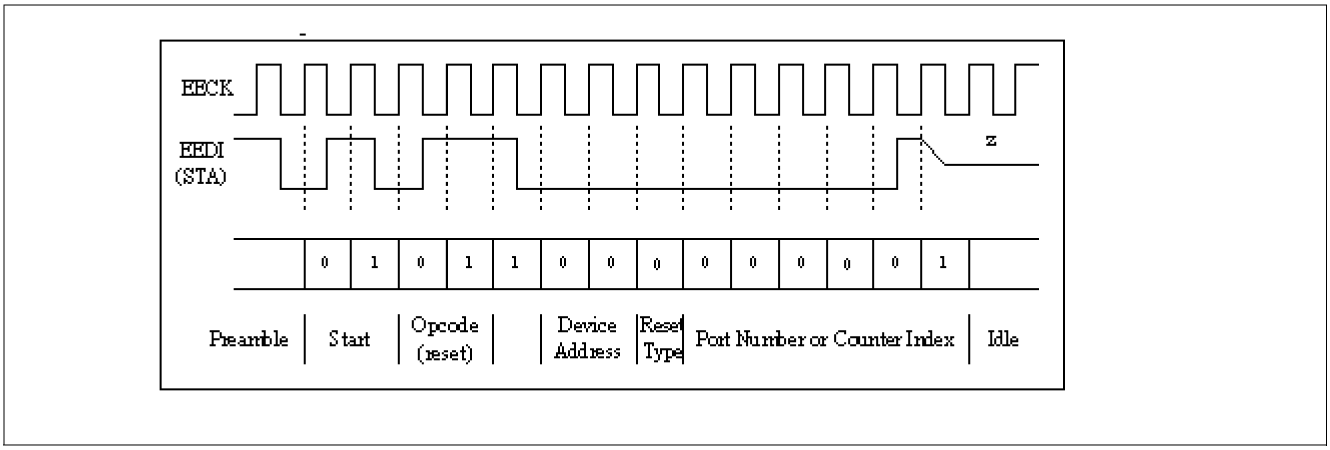

Figure 5 ADM6996L Issue Reset Internal Counter Command

Preamble: At least 32 continuous 1_B's

Start: 01_B(2 bits)

Opcode: 01_B (2 bits, Reset command)

Device Address: Chip physical address as PHYAS[1:0].

Reset_type: Reset the counter by port number or by counter index

1_B = Clear dedicate port's all counters

0_B = Clear dedicate counter

Port_number or counter index: User defines clear port or counter

Idle: EECK must send at least one clock pulse at idle time

5 Electrical Specification

5.1 TX/FX Interface

5.1.1 TP Interface

Transformer requirement:

- TX/RX rate 1:1
- TX/RX central tap connect together to VCCA2

Note: Users can change the TX/RX pin for easy layout but do not change polarity. The ADM6996L supports auto polarity on the receiving side

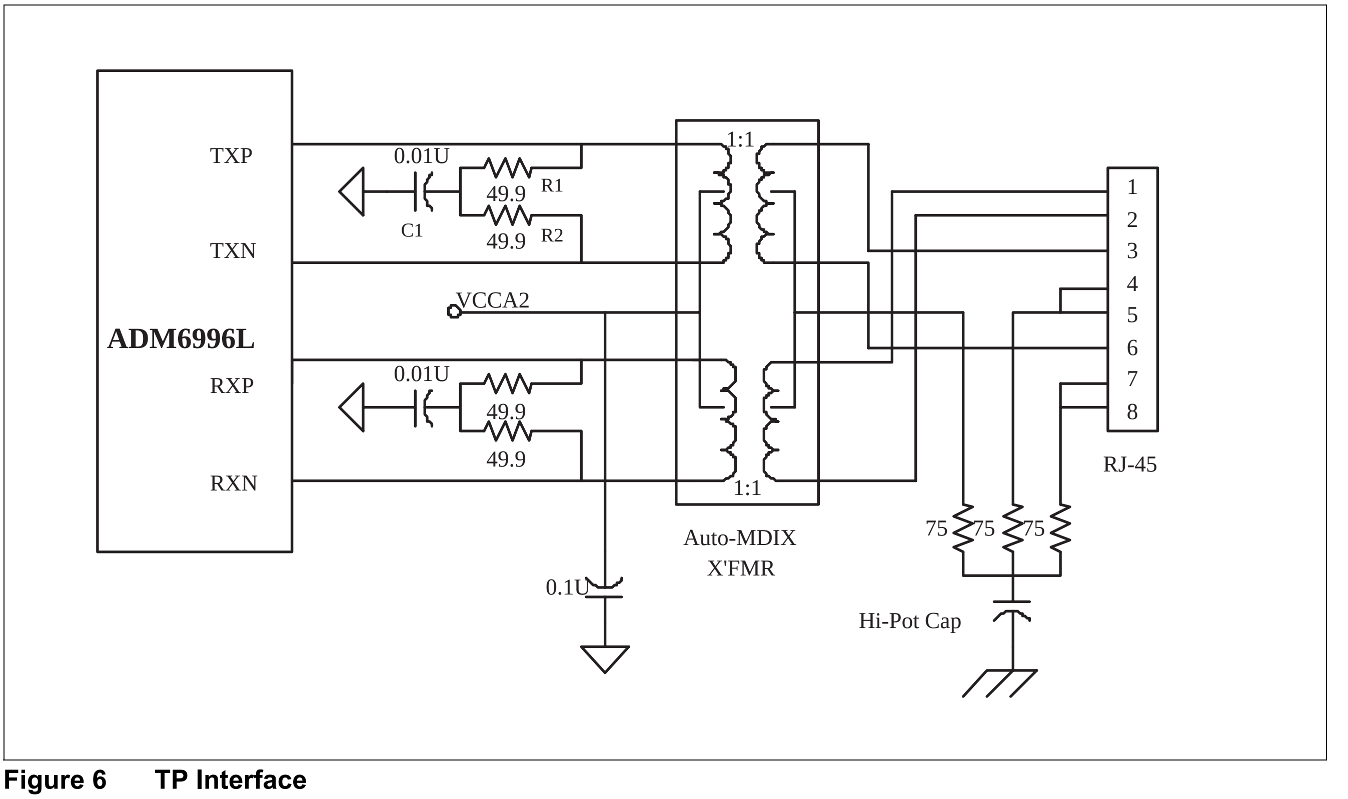

Figure 6 TP Interface

5.1.2 FX Interface

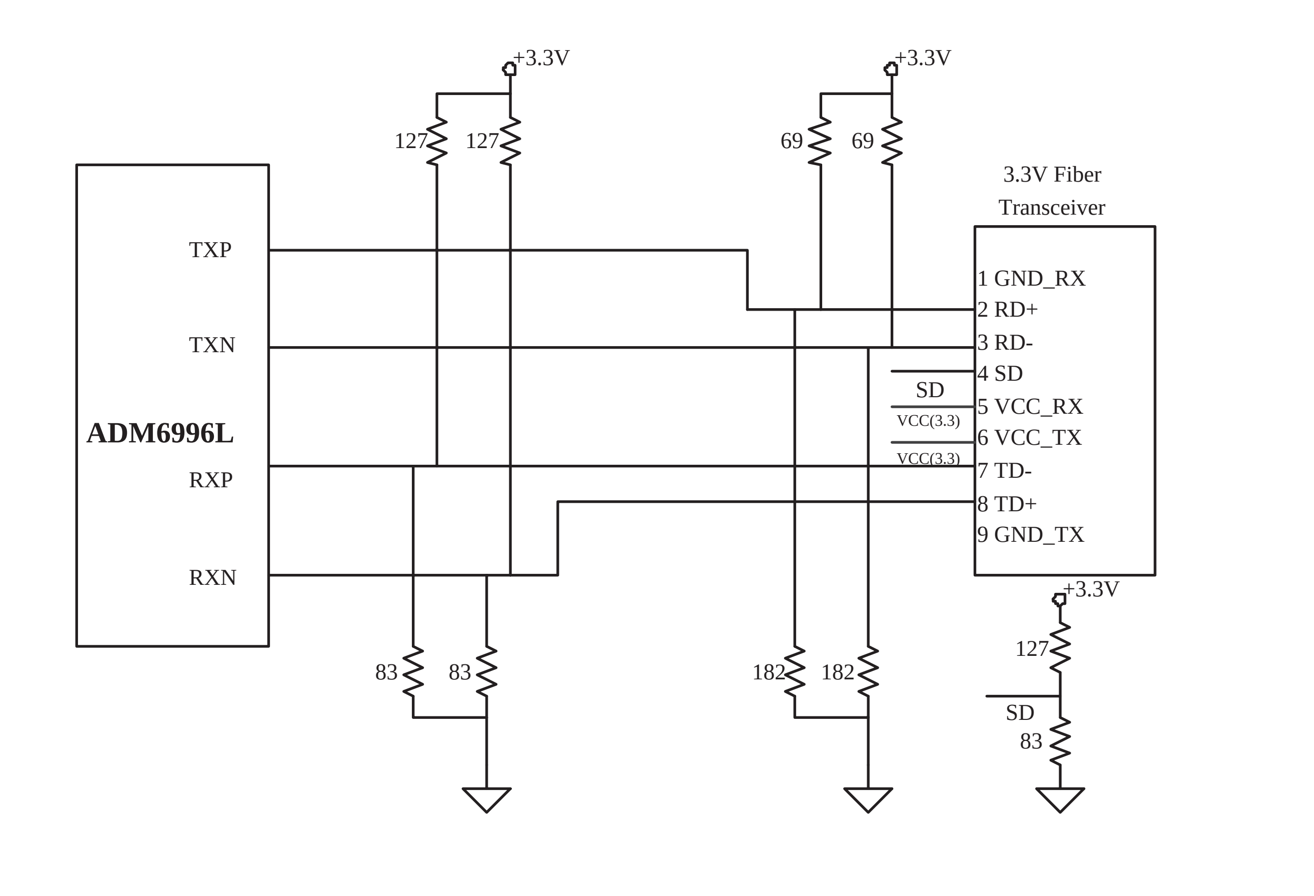

Figure 7 Fx Interface Layout

5.2 DC Characteristics

5.2.1 Absolute Maximum Rating

Table 26 Absolute Maximum Rating

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply	V_{CC}	-0.3		3.63	V	
TX line driver	*Vcca2*			1.8	V	
PLL voltage	*Vccpll*			1.8	V	
Digital core voltage	*Vccik*			1.8	V	
Input Voltage	V_{IN}	-0.3		V CC + 0.3	V	
Output Voltage	*Vout*	-0.3		Vcc + 0.3	V	
Storage Temperature	*TSTG*	-55		155	C	
Power Dissipation	*PD*			1.3W	W	
ESD Rating	*ESD*			2KV	V	

5.2.2 Recommended Operating Conditions

Table 27 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply	V_{cc}	2.8	3.3	3.465	V	
TX line driver	V_{cca2}	1.7	1.8	1.9	V	
PLL voltage	V_{ccpll}	1.7	1.8	1.9	V	
Digital core voltage	V_{ccik}	1.7	1.8	1.9	V	
Input Voltage	V_{in}	0	-	Vcc	V	
Power consumption	P_C		1.3		W	
Junction Operating Temperature	T_j	0	25	115	C	

5.2.3 DC Electrical Characteristics for 3.3 V Operation

Under Vcc=3.0 V~3.6 V, Tj= 0 C ~ 115 C

Table 28 DC Electrical Characteristics for 3.3 V Operation

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Low Voltage	V_{IL}			0.3 * Vcc	V	CMOS
Input High Voltage	V_{IH}	0.7 * Vcc			V	CMOS
Output Low Voltage	V_{OL}			0.4	V	CMOS
Output High Voltage	V_{OH}	0.7 * Vcc			V	CMOS
Input Pull_up/down Resistance	R_I		100		K	VIL=0 V or VIH = Vcc

Note: 100BaseT Full Duplex: 130mA (3.3 V) 500mA (1.8 V) => 1.329W

Note: 10BaseT Full Duplex: 50mA (3.3 V) 740mA (1.8 V) => 1.497W

Note: No Link: 30mA (3.3 V) 580mA (1.8 V) => 1.143W

5.3 AC Characteristics

5.3.1 Power On Reset

Describes what conditions are set when powered on

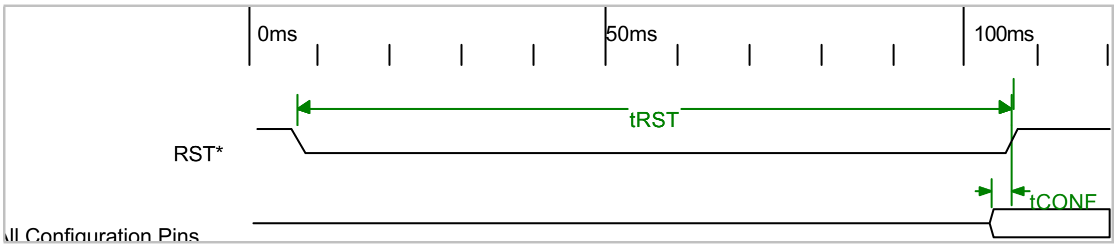

Figure 8 Power On Reset

Table 29 Power On Reset

Symbol	Parameter	Conditions	Min.	Typical	Max	Units
TRST	RST Low Period		100			Ms
TCONF	Start of Idle Pulse Width		100			Ns

5.3.2 EEPROM Interface Timing

Describes the EEPROM timing values

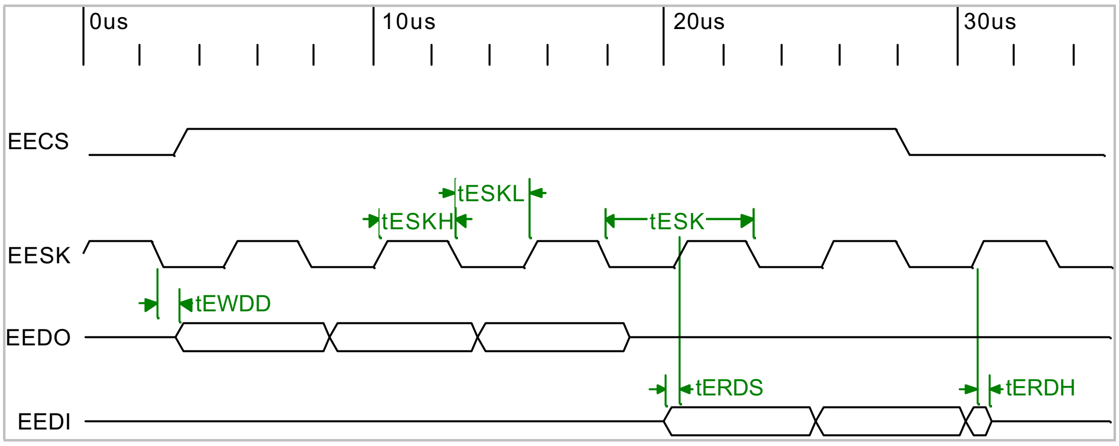

Figure 9 EEPROM Interface Timing

Table 30 EEPROM Interface Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Period	*tESK*		5120		ns	
EESK Low Period	*tESKL*	2550		2570	ns	
EESK High Period	*tESKH*	2550		2570	ns	

Table 30 EEPROM Interface Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EEDI to EESK Rising Setup Time	*tERDS*	10			ns	
EEDI to EESK Rising Hold Time	*tERDH*	10			ns	
EESK Falling to EEDO Output Delay Time	*tEWDD*			20	ns	

5.3.3 10Base-Tx MII Input Timing

10Base-Tx Input timing conditions

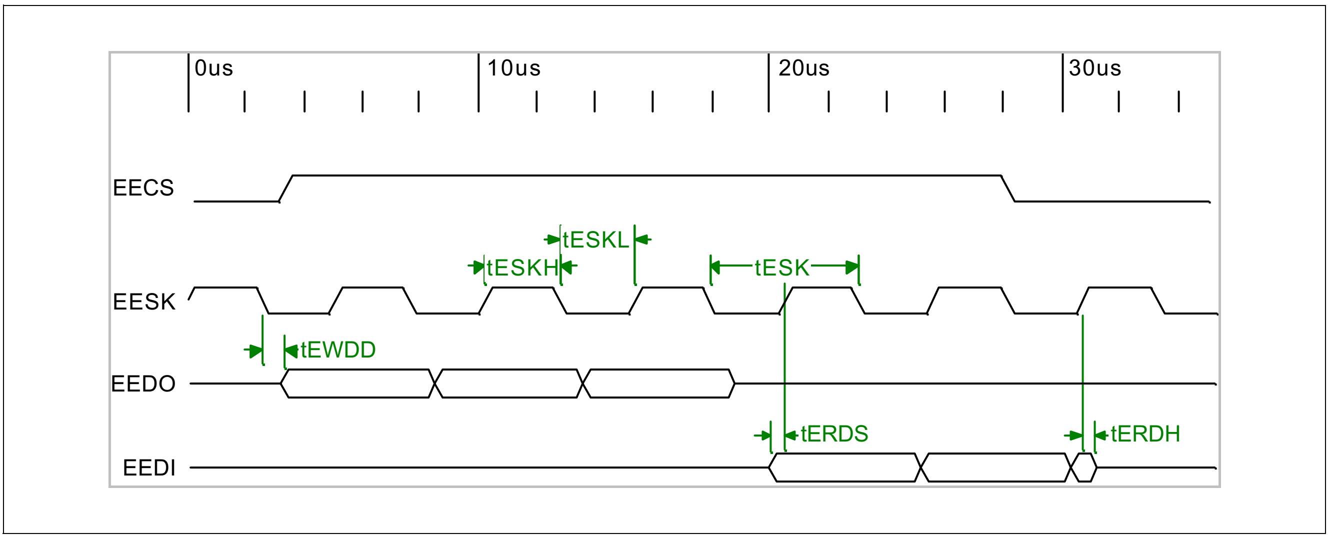

Figure 10 10Base-Tx MII Input Timing

Table 31 10Base-Tx MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	t_{CK}		400		ns	
MII_RXCLK Low Period	t_{CKL}	180		220	ns	
MII_RXCLK High Period	t_{CKH}	180		220	ns	
MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising setup	t_{RXS}	10			ns	
MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising hold	t_{RXH}	10			ns	

5.3.4 10Base-TX MII Output Timing

10Base-TX MII Output timing conditions

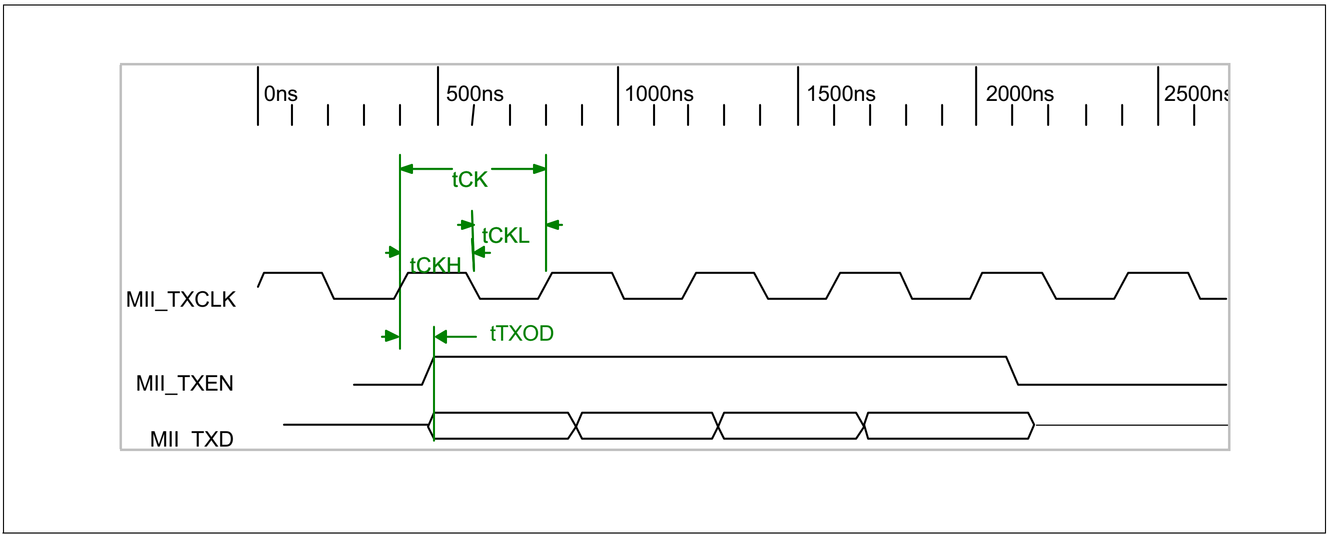

Figure 11 10Base-TX MII Output Timing

Table 32 10Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	*tCK*		400		ns	
MII_TXCLK Low Period	*tCKL*	180		2 20	ns	
MII_TXCLK High Period	*tCKH*	1 80		220	ns	
MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay	*tTXOD*	0		25	ns	

5.3.5 100Base-Tx MII Input Timing

100Base Tx MII Input timing conditions

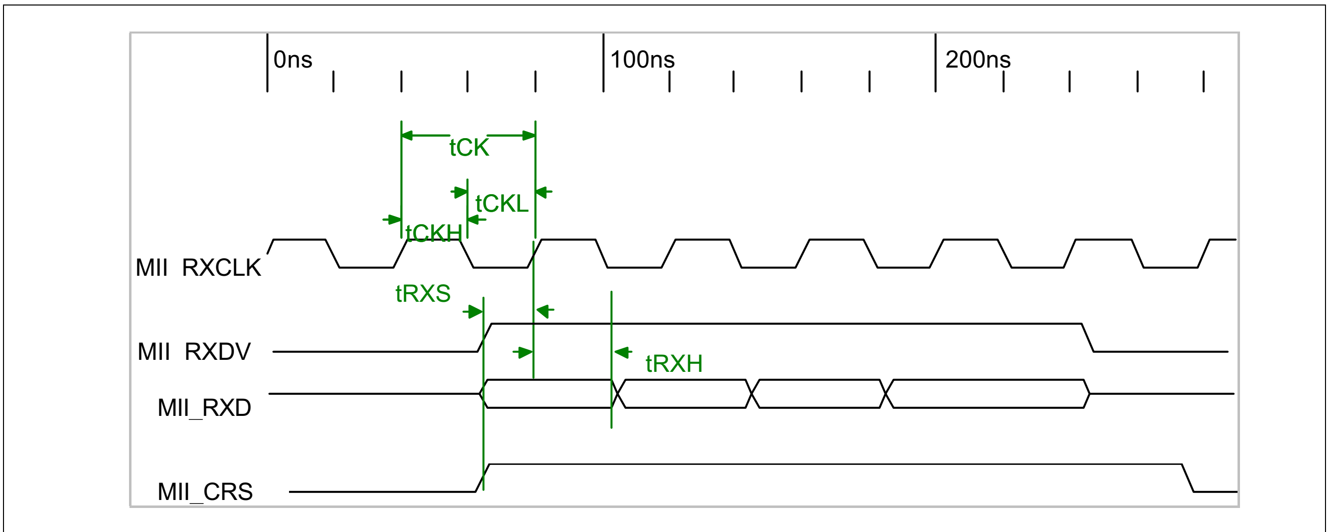

Figure 12 100Base-TX MII Input Timing

Table 33 100Base-TX MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	*tCK*		40		ns	
MII_RXCLK Low Period	*tCKL*	1 8		22	ns	
MII_RXCLK High Period	*tCKH*	1 8		22	ns	
MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising setup	*tRXS*	10			ns	
MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising hold	*tRXH*	10			ns	

5.3.6 100Base-TX MII Output Timing

100Base-TX MII Output timing conditions

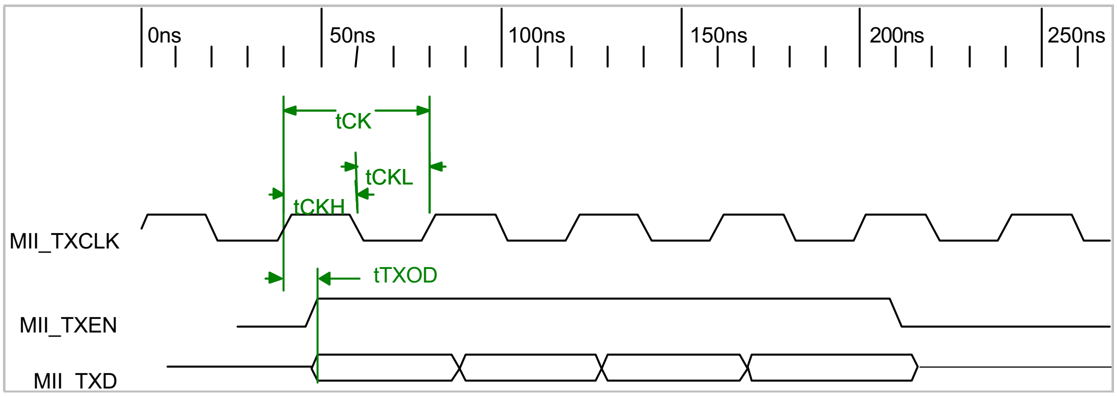

Figure 13 100Base-TX MII Output Timing

Table 34 100Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	*tCK*		40		ns	
MII_TXCLK Low Period	*tCKL*	1 8		22	ns	
MII_TXCLK High Period	*tCKH*	18		22	ns	
MII_TXD, MII_TXEN to MII_TXCLK Rising Out put Delay	*tTXOD*	0		25	ns	

5.3.7 GPSI(7-wire) Input Timing

GPSI (7-wire) Input timing conditions

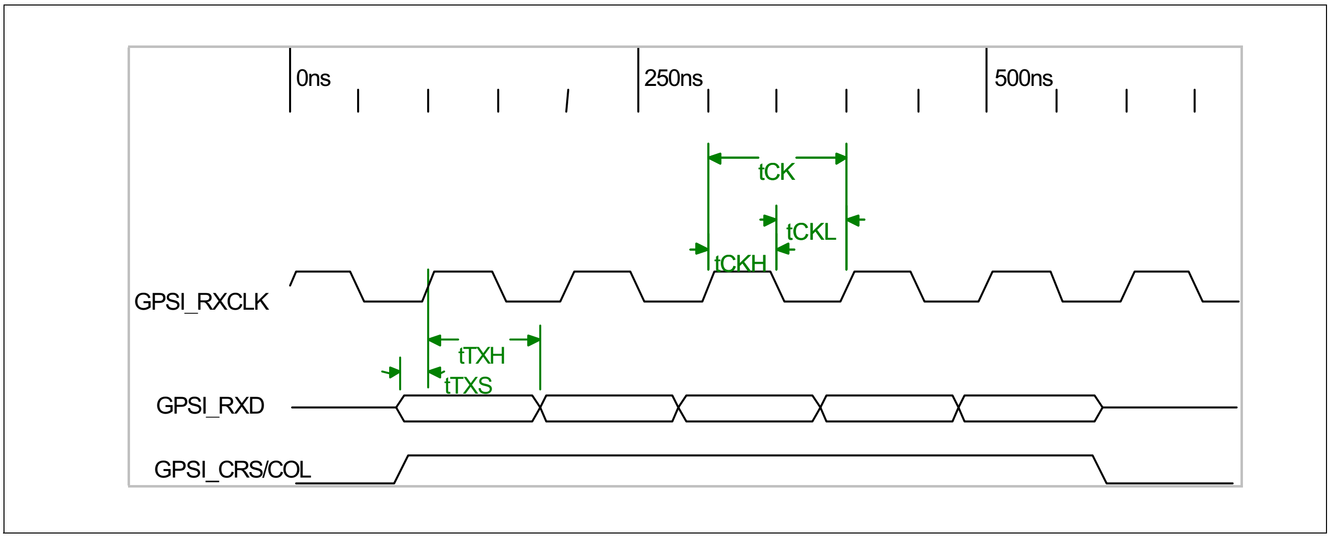

Figure 14 GPSI(7-wire) Input Timing

Table 35 GPSI (7-wire) Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GPSI_RXCLK Period	*tCK*		100		ns	
GPSI_RXCLK Low Period	*tCKL*	40		60	ns	
GPSI_RXCLK High Period	*tCKH*	40		60	ns	
GPSI_RXD, GPSI_CRS /COL to GPSI_RXCLK Rising Setup Time	*tTXS*	10			ns	
GPSI_RXD, GPSI_ CRS/COL to GPSI_RXCLK Rising Hold Time	*tTXH*	10			ns	

5.3.8 GPSI (7-wire) Output Timing

GPSI (7-wire) Output timing conditions

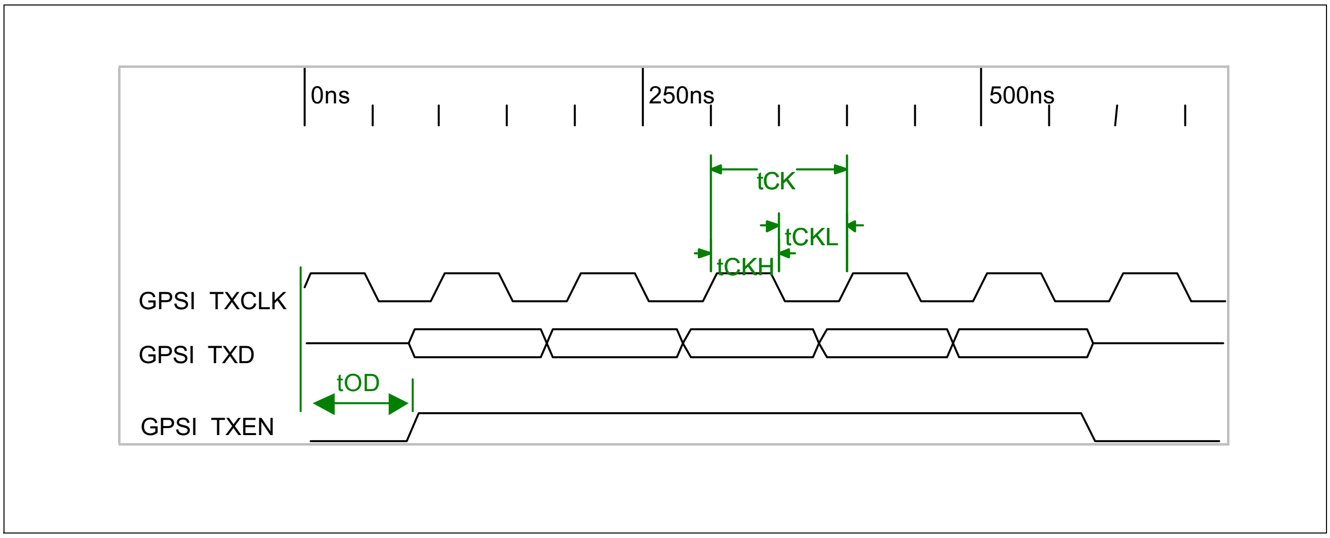

Figure 15 GPSI (7-wire) Output Timing

Table 36 GPSI (7-wire) Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GPSI_TXCLK Period	*tCK*		100		ns	
GPSI_TXCLK Low Period	*tCKL*	40		60	ns	
GPSI_ T XCLK High Period	*tCKH*	40		60	ns	
GPSI_ T XCLK Rising to GPSI_TXEN/GPSI_TXD Output Delay	*tOD*	50		70	ns	

6 Packaging

This chapter describes the ADM6996L's packaging.

6.1 128 Pin PQFP Outside Dimension

ADM6996L packaging

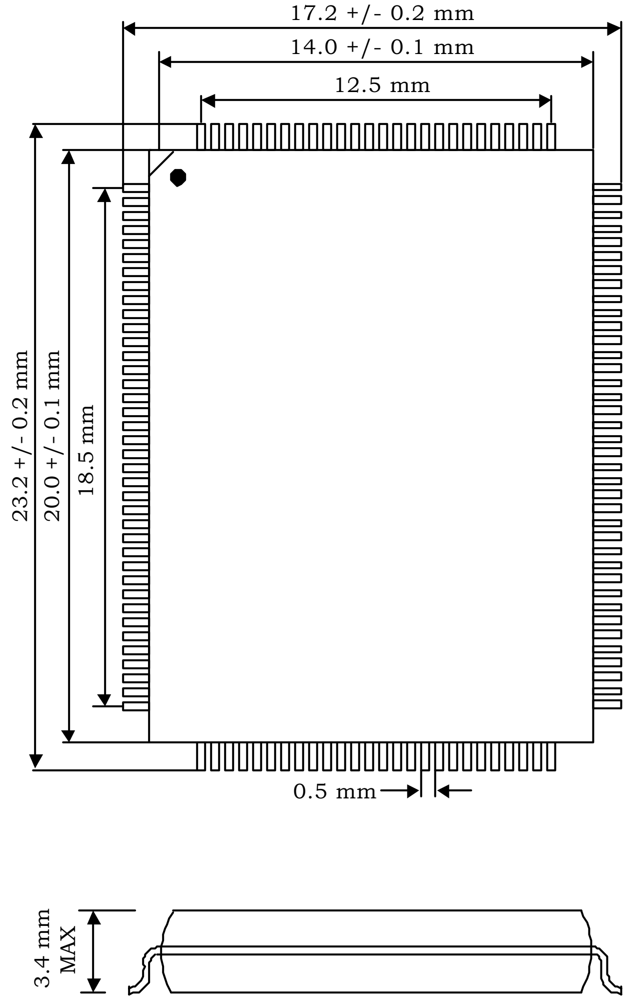

Figure 16 128-pin LQFP Chip Package

TerminologyTerminology

A

B

w w w . i n f i n e o n . c o m

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